Section 19. Dual Comparator Module

HIGHLIGHTS

This section of the manual contains the following major topics:

19.1 INTRODUCTION

The analog dual comparator module contains two comparators that can be configured in a variety of ways. The inputs can be selected from the analog inputs multiplexed with the I/O pins, as well as the on-chip voltage reference (see **Section 20. "Comparator Voltage Reference Module"**). Block diagrams of the various comparator configurations are shown in Figure 19-1.

Note:	A comparator module with two analog comparators may also be the scalable comparator module, described in the *"PIC24F Family Reference Manual"*, **Section 46. "Scalable Comparator Module"** (DS39734). Check the device data sheet to verify which comparator module is included in a particular device.

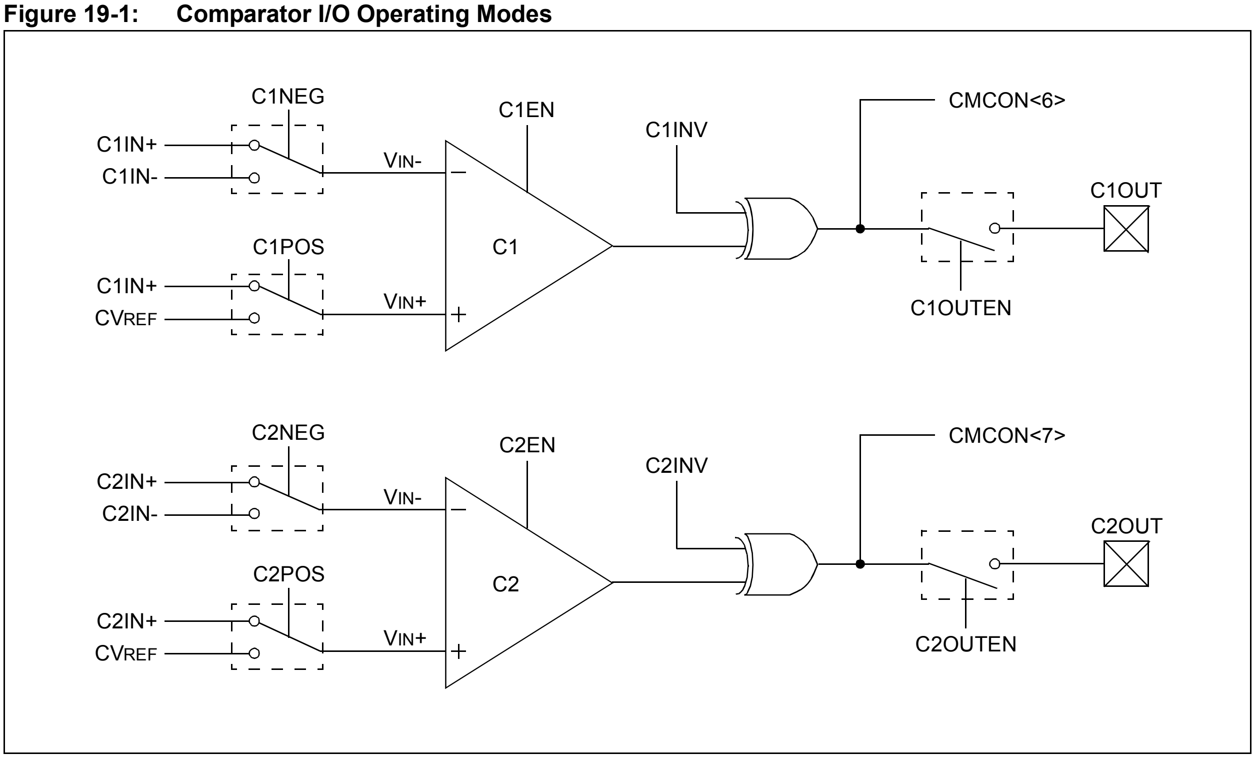
19.1.1 Comparator Configuration

PIC24F devices offer near 100% flexibility in configuration of the comparator module, allowing individual control over many of the options that are fixed on most PIC18 devices. The PIC24F comparator module has individual control over the enables, output inversion, output on I/O pin and input selections. The V_{IN-} pin of each comparator can select from either I/O pin (CxIN+ or CxIN-) and the V_{IN+} input of the comparator comes from the comparator voltage reference, or the positive I/O pin (CxIN+ or CV_{REF}). In addition, the PIC24F has 2 individual comparator event control bits. These control bits can be used for detecting when an individual comparator output changes states.

If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay.

Note:	Comparator interrupts should be disabled during a Comparator mode change; otherwise, a false interrupt may occur.

Figure 19-1: Comparator I/O Operating Modes



19.2 CONTROL REGISTER

The CMCON register (Register 19-1) is used to configure the comparator and present their output status. The C2EN and C1EN bits (CMCON<11:10>) enable or disable the individual comparators.

Comparator input configuration is accomplished with the CxNEG and CxPOS bits (CMCON<3:0>). These determine which of the differential input channels is connected to the non-inverting input, and if either a differential comparator input or the comparator voltage reference is connected to the inverting input. A total of 16 possible configurations are available for both comparators.

The CxOUT bits (CMCON<7:6>) directly report the output state of the comparator, as determined by the relative values of Vin+ and Vin-, and the CxINV bits (CMCON<5:4>). The CxOUTEN bits (CMCON<9:8>) enable the output of the comparator to appear on the corresponding CxOUT pin. The CxEVT pins (CMCON<13:12>) indicate when any change in output state has occurred. These bits are set by hardware and can only be cleared in software.

Register 19-1: CMCON: Comparator Control Register

R/W-0	U-0	R/C-0	R/C-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIDL	—	C2EVT	C1EVT	C2EN	C1EN	C2OUTEN	C1OUTEN
bit 15							bit 8

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	C2NEG	C2POS	C1NEG	C1POS
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL:** Stop in Idle Mode bit
1 = When device enters Idle mode, the module does not generate interrupts; the module is still enabled
0 = Continue normal module operation in Idle mode

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **C2EVT:** Comparator 2 Event bit
1 = Comparator output changed states
0 = Comparator output did not change states

bit 12 **C1EVT:** Comparator 1 Event bit
1 = Comparator output changed states
0 = Comparator output did not change states

bit 11 **C2EN:** Comparator 2 Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 10 **C1EN:** Comparator 1 Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 9 **C2OUTEN:** Comparator 2 Output Enable bit
1 = Comparator output is driven on the output pad
0 = Comparator output is not driven on the output pad

bit 8 **C1OUTEN:** Comparator 1 Output Enable bit
1 = Comparator output is driven on the output pad
0 = Comparator output is not driven on the output pad

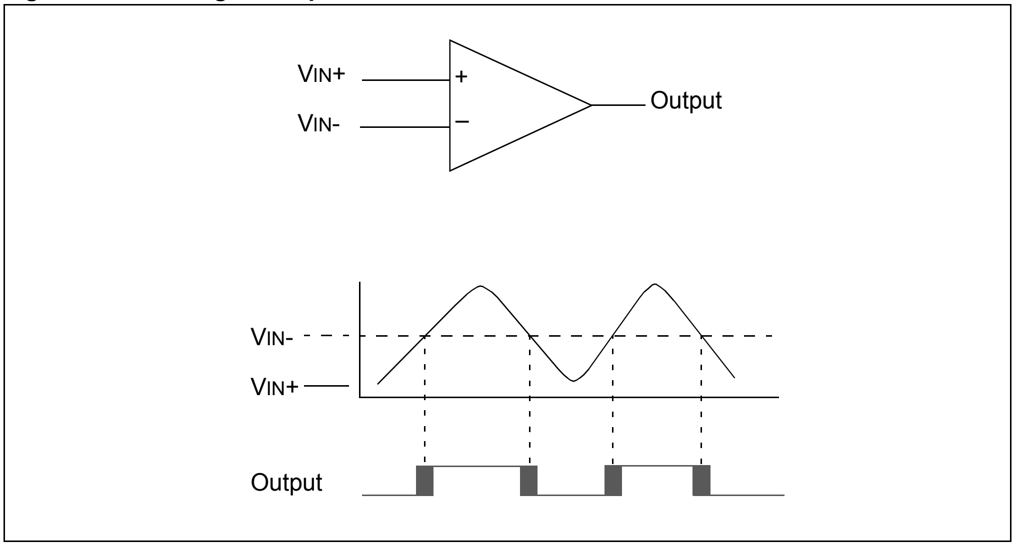
Register 19-1: CMCON: Comparator Control Register (Continued)

bit 7	**C2OUT:** Comparator 2 Output bit When C2INV = `0`: `1` = C2IN+ > C2IN- `0` = C2IN+ < C2IN- When C2INV = `1`: `0` = C2IN+ > C2IN- `1` = C2IN+ < C2IN-
bit 6	**C1OUT:** Comparator 1 Output bit When C1INV = `0`: `1` = C1IN+ > C1IN- `0` = C1IN+ < C1IN- When C1INV = `1`: `0` = C1IN+ > C1IN- `1` = C1IN+ < C1IN-
bit 5	**C2INV:** Comparator 2 Output Inversion bit `1` = C2 output is inverted `0` = C2 output is not inverted
bit 4	**C1INV:** Comparator 1 Output Inversion bit `1` = C1 output is inverted `0` = C1 output is not inverted
bit 3	**C2NEG:** Comparator 2 Negative Input Configure bit `1` = Input is connected to C2IN+ `0` = Input is connected to C2IN- See Figure 19-1 for the Comparator modes.
bit 2	**C2POS:** Comparator 2 Positive Input Configure bit `1` = Input is connected to C2IN+ `0` = Input is connected to CVREF See Figure 19-1 for the Comparator modes.
bit 1	**C1NEG:** Comparator 1 Negative Input Configure bit `1` = Input is connected to C1IN+ `0` = Input is connected to C1IN- See Figure 19-1 for the Comparator modes.
bit 0	**C1POS:** Comparator 1 Positive Input Configure bit `1` = Input is connected to C1IN+ `0` = Input is connected to CVREF See Figure 19-1 for the Comparator modes.

19.3 COMPARATOR OPERATION

A single comparator is shown in Figure 19-2, along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input, VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 19-2 represent the uncertainty due to input offsets and response time.

Figure 19-2: Single Comparator



19.4 COMPARATOR REFERENCE

Depending on the comparator operating mode, either an external or internal voltage reference may be used. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly (Figure 19-2).

19.4.1 External Reference Signal

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same, or different, reference sources. However, threshold detector applications may require the same reference.

19.4.2 Internal Reference Signal

The comparator module also allows the selection of an internally generated voltage reference from the comparator voltage reference module. This module is described in more detail in **Section 20. "Comparator Voltage Reference Module"**.

The internal reference is available when C1POS = `0`, C2POS = `0` and the CVRSS bit (CVRCON<4>) = `0`. In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

19.5 COMPARATOR RESPONSE TIME

Response time is the maximum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used.

19.6 COMPARATOR OUTPUTS

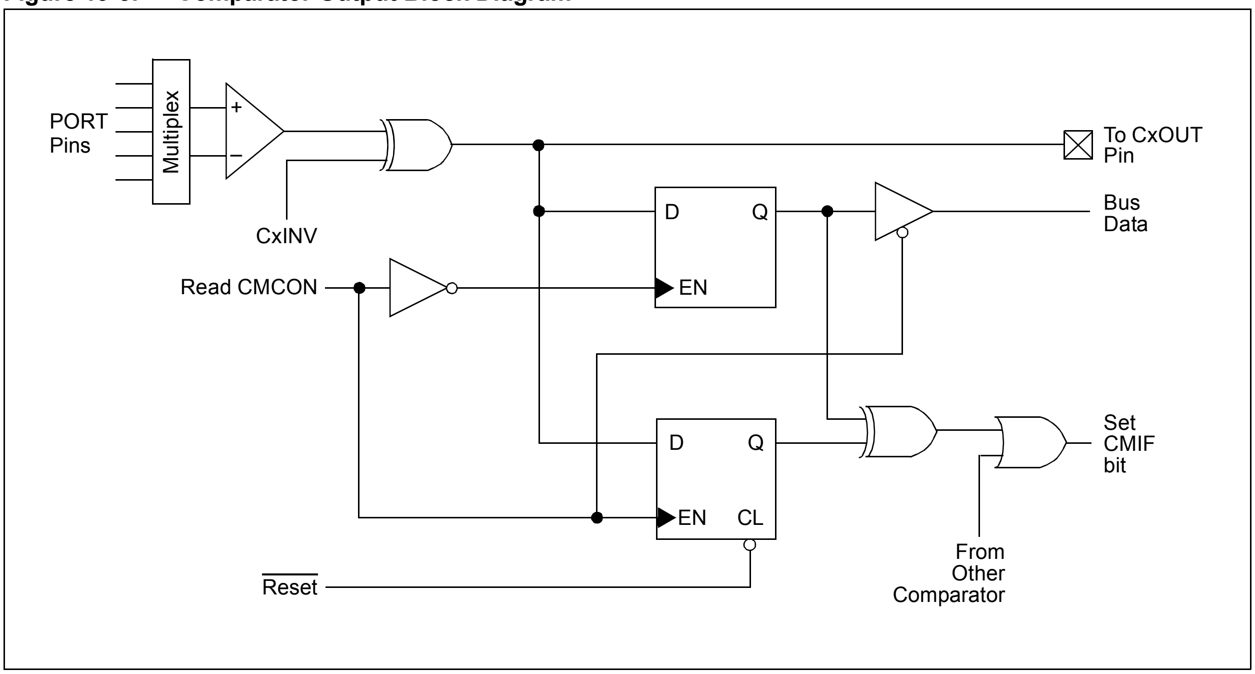
The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the I/O pins via C1OUT and C2OUT. When enabled, multiplexers in the output path of the I/O pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 19-3 shows the comparator output block diagram.

The associated TRIS bits will still function as an output enable/disable for the I/O pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<5:4>).

> **Note 1:** When reading the PORT register, all pins configured as analog inputs will read as '`0`'s. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
>
> **2:** Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

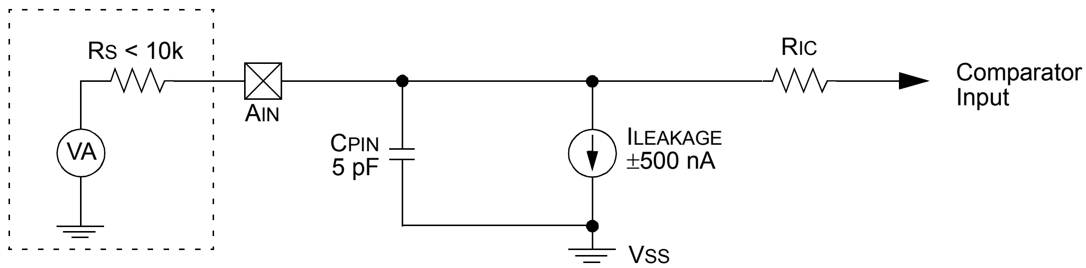
Figure 19-3: Comparator Output Block Diagram



19.7 ANALOG INPUT CONNECTION CONSIDERATIONS

A simplified circuit for an analog input is shown in Figure 19-4. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

Figure 19-4: Comparator Analog Input Model



Legend:			
	CPIN	=	Input Capacitance
	ILEAKAGE	=	Leakage Current at the pin due to various junctions
	RIC	=	Interconnect Resistance
	RS	=	Source Impedance
	VA	=	Analog Voltage

19.8 INITIALIZATION

This initialization sequence configures the comparator module as two independent comparators with outputs enabled and the Comparator 1 output inverted. The comparator voltage reference module is configured for output enable and set for 0.25 * V_{DD}. Example 19-1 shows a program sequence to configure the voltage reference and comparator module. The delay used in this example is based off of an 8 MHz oscillator.

Example 19-1: Comparator Configuration

```
CMCON          = 0x0F10;          //Initialize Comparator Module

CVRCON         = 0x00C0;          //Initialize Voltage Reference Module

CMCONbits.C1EVT = 0;              //Clear Comparator 1 Event
CMCONbits.C2EVT = 0;              //Clear Comparator 2 Event

asm volatile("repeat #40");       //Delay 10us
Nop();
```

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Dual Comparator Module

19.9 COMPARATOR INTERRUPTS

The Comparator Interrupt Flag, CMIF (IFS1<2>), is set whenever there is a change in the output value of either comparator. Software can read C1EVT and C2EVT to determine the actual change that occurred. Since it is also possible to write a '`1`' to this register, a simulated interrupt may be initiated. The CMIF and CxEVT bits must be reset by clearing them in software.

If the CMIE bit (IEC1<2>) is cleared, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note:	If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (IFS1<2>) interrupt flag may not get set.

The user, in the Interrupt Service Routine, can clear the interrupt by clearing CMIF. See **Section 8. "Interrupts"** in this manual for more information.

19.10 COMPARATOR OPERATION DURING SLEEP AND IDLE MODES

19.10.1 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake-up the device from Sleep mode, when enabled. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in Sleep mode, turn off the comparators, CxEN = `0` (CMCON<11:10>), before entering Sleep. If the device wakes up from Sleep, the contents of the CMCON register are not affected. See **Section 10. "Power-Saving Features"** in this manual for additional information on Sleep.

19.10.2 Comparator Operation During Idle

When a comparator is active and the device is placed in Idle mode, the comparator remains active and interrupts are generated, if enabled, and CMIDL = `0` (CMCON<15>). If it is desired for the comparators to operate in Idle mode without generating interrupts, configure CMIDL = `1` (CMCON<15>). See **Section 10. "Power-Saving Features"** in this manual for more information on Idle.

19.11 EFFECTS OF A RESET

A device Reset forces the CMCON register to its Reset state, causing the comparator modules to be turned off (CxEN = `0`). However, the input pins multiplexed with analog input sources are configured as analog inputs, by default, on device Reset. The I/O configuration for these pins is determined by the setting of the ADxPCFG register. Therefore, device current is minimized when analog inputs are present at Reset time.

19.12 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator module are:

Title	Application Note #
Resistance and Capacitance Meter Using a PIC16C622	AN611
Make a Delta-Sigma Converter Using a Microcontroller's Analog Comparator Module	AN700
A Comparator Based Slope ADC	AN863
Oscillator Circuits for RTD Temperature Sensors	AN895
Temperature Measurement Circuits for Embedded Applications	AN929
Analog Sensor Conditioning Circuits – An Overview	AN990

> **Note:** Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

19.13 REVISION HISTORY

Revision A (June 2006)

This is the initial released revision of this document.

Revision B (March 2010)

Renamed as "Dual Comparator Module", to distinguish from the recently introduced **Section 46. "Scalable Comparator Module"** (DS39734).

Reorganized all topics to reflect the order used in **Section 46. "Scalable Comparator Module"**. Replaced the text of **Section 19.2 "Control Register"** with a new version, to provide a clearer explanation of the register.

Revised Figure 19-3 to correct the "Read CMCON" circuit input.

Revised Figure 19-4 with an updated input model.

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