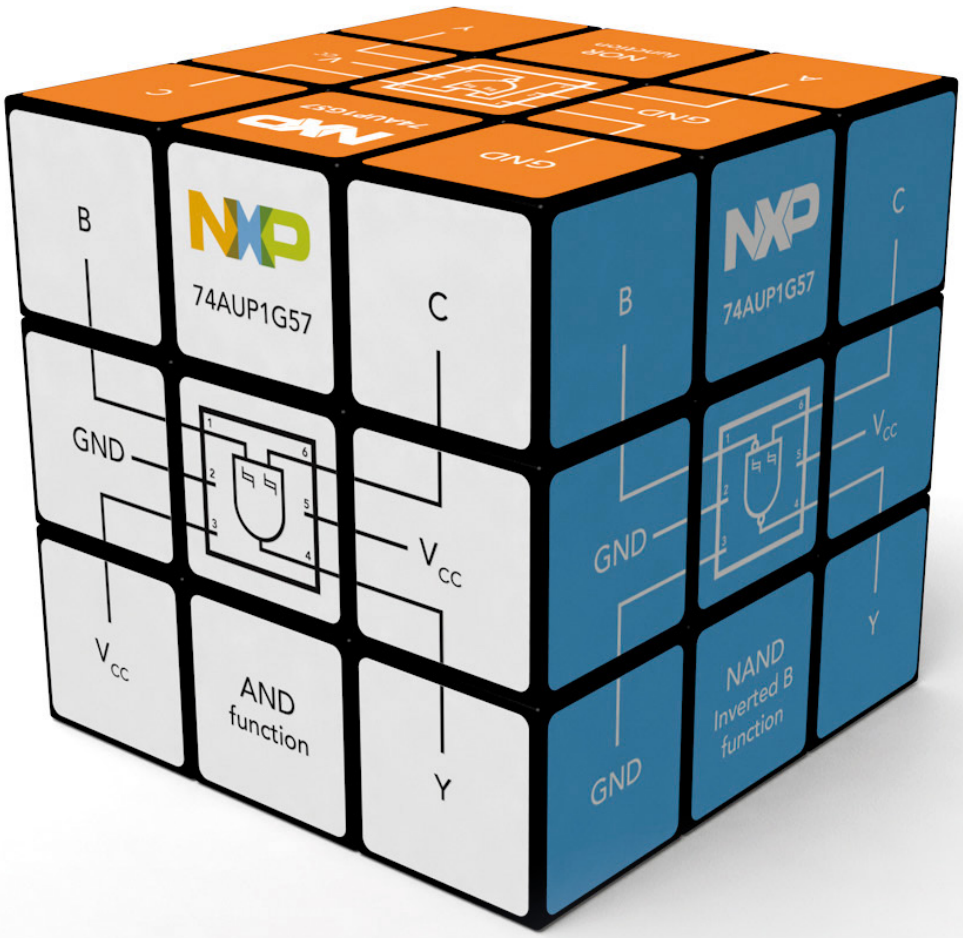
Logic selection guide 2016

Standard Logic and Mini Logic in leaded and leadless packages


B
NXP
74AUP1G57
C
GND
V_{CC}
V_{CC}
AND
function
Y
B
NXP
74AUP1G57
C
GND
V_{CC}
GND
NAND
Inverted B
function
Y

Standard Logic and Mini Logic: tuned for today's systems

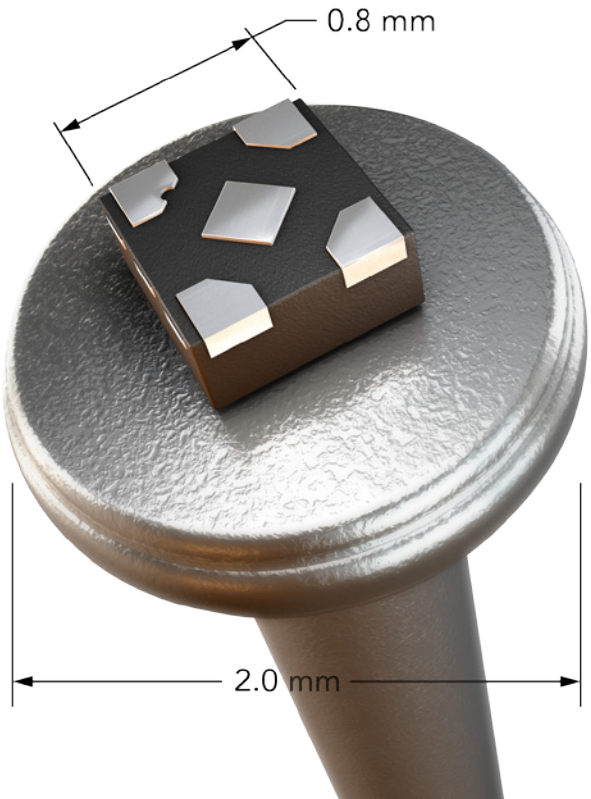
Logic may have been around since the days when engineers still used slide rules, but logic is still an essential part of embedded design.

It's the go-to resource for I/O expansion and interfacing between analog and digital domains, but that's just the beginning. In many ways, today's designers need logic more than ever. Why? Because today's systems need to be smaller, more power efficient, and more portable than ever before. That means managing tight layouts, and dealing with looped traces, which can generate cross-talk and create signal-integrity issues. It also means working with multi-layer boards, implementing real-time responses to real-world events, and supporting multi-tasking operations. In many cases, the right logic device makes these things easier to manage, and helps optimize operation.

Here are just some of the ways that Standard and Mini Logic works in today's embedded systems:

- Enables quick reconfiguration, by adding gates outside the core logic or MCU, for selection of debugging and functional modes
- Provides the interface between peripherals, by performing level translation, reset control, power sequencing, signal switching, signal isolation, and so on
- Uses low-power functions to add new features without overtaxing the battery
- Enables the integration of touchscreens and touchpads with multiplexers, shifters, and latches
- Implements video switching between different displays and video formats by doing format conversion, adapting interfaces to controllers, and multiplexing/demultiplexing the connectors
- Extends GPIO and drives LEDs
- Supports automotive applications by implementing simple motor control, smart key detection, security alarms, speed alerts, and more

Table of contents



Where logic really stands out

Logic is great for making minor modifications and fine-tuning performance in the later design stages, but that's not all it can do. Today's logic devices let you add features and improve functionality, so you can meet your design requirements right from the start, even before you need to think about last-minute revisions.

ASIC-driven systems

In systems that use application-specific integrated circuits (ASICs), logic gates can be used to provide control or "glue" functions. Modern logic families include features, such as overvoltage tolerance, that enable them to be used as glue logic between ASICs that use different supply voltages. In some cases, this can extend the lifetime of legacy ASICs. Available in small-footprint packages, such as PicoGate, MicroPak, and Diamond, today's glue logic is suitable for space-constrained applications.

MCU-driven systems

In systems that use a microcontroller (MCU), logic products are used for low-cost I/O expansion. Shift registers are used for digital I/O expansion, and analog switches are used to multiplex analog sensor inputs. The combination of the two enables the selection of lower-pincount MCUs with fewer analog-to-digital converters. When used this way, standard logic enables true cost optimization of an application. Dual supply-voltage translators make it possible to use MCU-based systems across multiple supply-voltage domains.

Computing

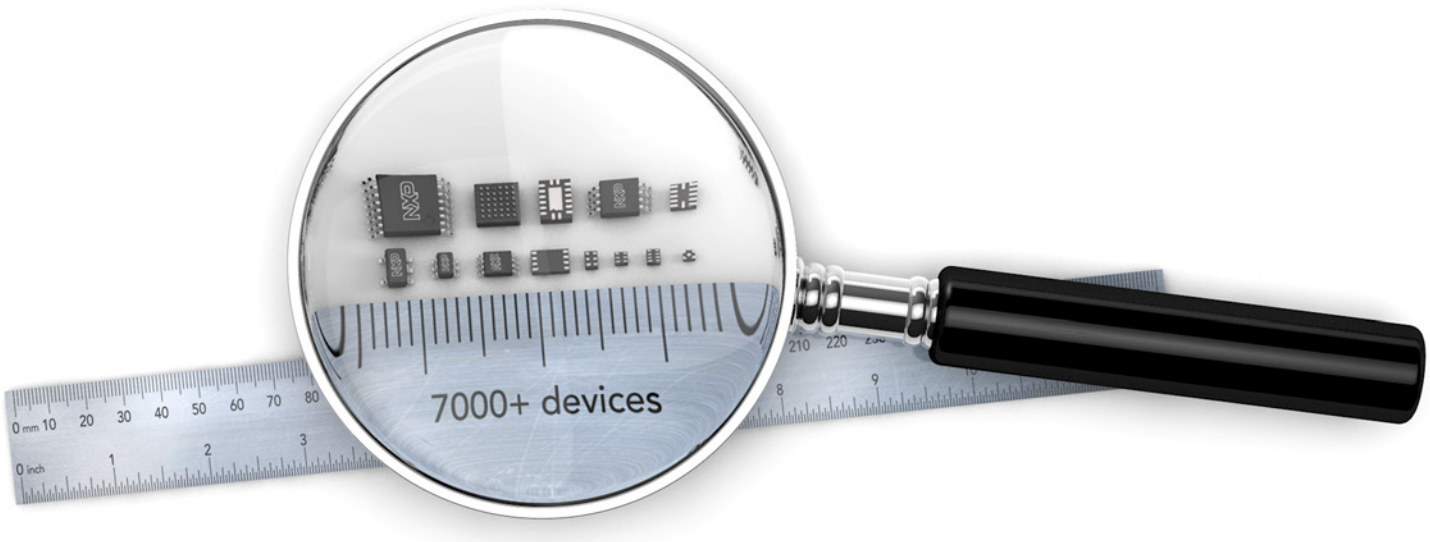
In tablets and laptops, logic can be used for battery charging and discharging blocks, and to provide standby mode, power-down, and start-up control sequences. In docking stations and systems that support multiple displays, logic provides the bus switches, resets, and audio blocks that reduce the impact of noisy signals, and can be used to buffer the clock and data signals.

Mobile

In mobile devices such as smartphones, tablets, and cameras, logic provides multiplexing, buffering, and level-translation functions for the baseband, RF interfaces, memory, and other peripherals.

Audio

Logic buffers are used in external speakers and other high-end audio equipment to buffer the clock, sync, and data signals sent to the audio interface and docking station.



NXP is the #1 volume leader

For the last 50 years, NXP's logic business has supported the growing global demand for logic. Today, as the No. 1 volume logic supplier, we offer a remarkably broad portfolio of cutting-edge solutions and best-in-class packages. Add this to our ability to support high-volume requirements, and our reputation as a trusted supplier of exceptionally high quality, and NXP is the logical choice as a partner for the long term.

Selection

We offer thousands of products, so it's easier to find what you want, when you want it. You can be certain that our portfolio has just the right combination of functions, packages, and operating voltages. We also offer special features that make your work easier, by simplifying design, increasing performance, adding flexibility, or all of the above.

Innovation

Logic continues to evolve, and that means our portfolio does, too. We consistently deliver new ideas, whether it's higher integration, lower power, smaller packaging, or just a better way to do things. Combination logic, for example, provides more than one function in a single package, so you can do more with a single inventory item. Another example is configurable logic, which lets you use a single package to configure up to nine different functions. The benefits are better system performance with a lower bill of materials, and a smaller board.

Packaging

We are a recognized leader in packaging technology, and offer the industry's largest portfolio of logic functions in leadless DQFN, MicroPak, and Diamond packages. That includes more than 50 leadless packages, all of which are qualified for use in automotive applications. And, while we offer a wide range of the latest leadless formats, we also understand that legacy packages, like SO and TSSOP, still have their place in some designs. We continue to support these older formats, so you can be confident that, whichever package you select, it will be available for as long as you need it.

Voltages

Today's systems often include products that work at different operating voltages, and there's no single voltage that works for every system. We offer a wide variety of operating voltages to choose from, so you can simplify your selection process and improve system performance. Look for coverage in both the low and the high end of the operating range, from 0.8 to 5 V and beyond.

Ruggedness

If you're designing a system that needs to perform in rugged environments, our many products that conform to the automotive standard AEC-Q100 can help you meet the necessary requirements. Our automotive logic devices have been verified to perform at higher temperatures, and can be counted on to provide reliable operation in tough situations.

Commitment

Having a partner you can count on makes it easier to meet deadlines and complete designs. At NXP, we are fully committed to the logic market and continue to invest in new process technologies, new packaging technologies, and new manufacturing facilities. These are the things that keep our portfolio competitive, and ensure our longevity as technology partner.

Combination and configurable logic

NXP's combination and configurable logic devices make it possible to do more with less, because they give you more ways to implement the "glue" logic functions commonly found in today's complex systems. These flexible and innovative single-package solutions let you replace discrete logic solutions with a configurable or combination logic device, so you can potentially reduce pin count, device count, system cost, and assembly-related expenses. These devices can also simplify inventory control and reduce qualification effort, since there are fewer discrete logic devices to deal with.

What is combination logic?

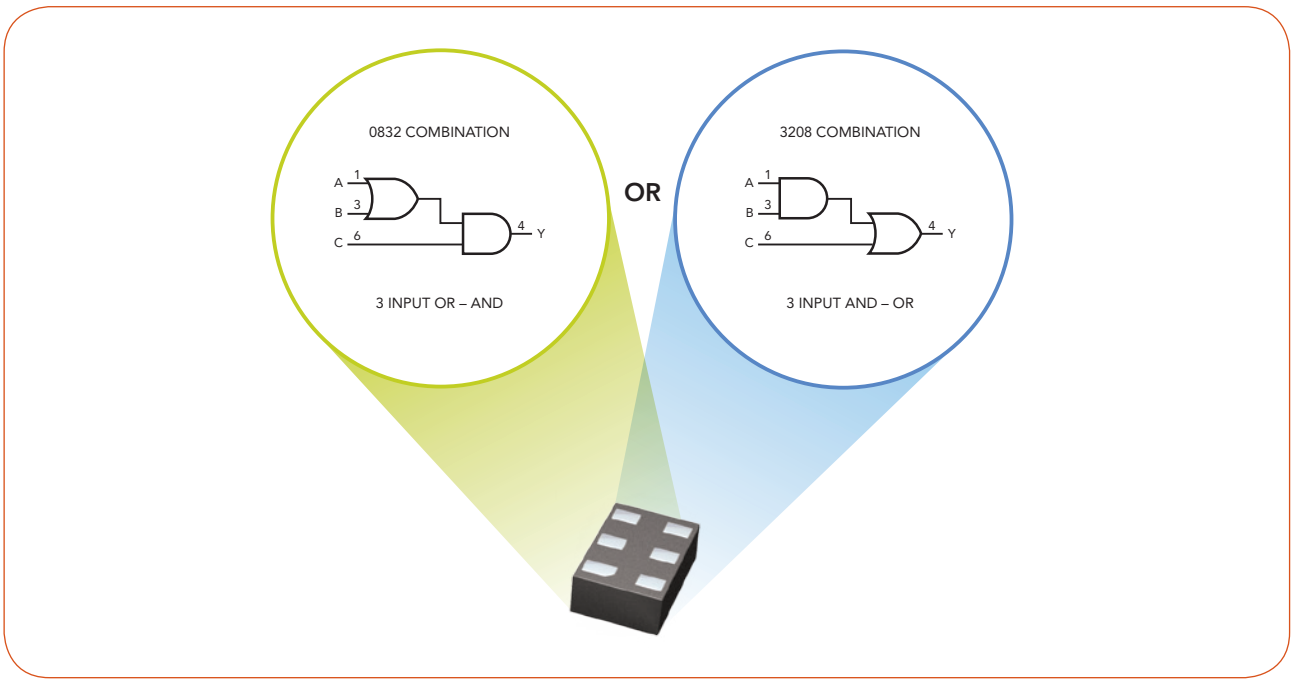
Combination logic places two or more dissimilar functions in a single package. The functions can either be internally cascaded or fully independent.

Benefits of combination logic

Combination logic reduces the number of components in the bill of materials (BOM), and that improves logistics, makes pick-and-place operations more efficient, and lowers the cost of assembly. Combining functions also reduces the footprint of the solution and, if the devices are internally cascaded, simplifies the PCB layout.

Learn more:

www.nxp.com/logic



Combination logic = one package, two or more different functions

What is configurable logic?

Configurable logic places up to nine functions in a single package. These functions include 2-input AND, OR, NAND, NOR, XOR, or XNOR gates, plus inverters and buffers, and a 2:1 mux. The logic function is selected by connecting input pins to either GND or V_{CC}. Schmitt-trigger inputs are standard. Low input-threshold options are included in NXP's portfolio, to interface between different supply-voltage domains.

Benefits of configurable logic

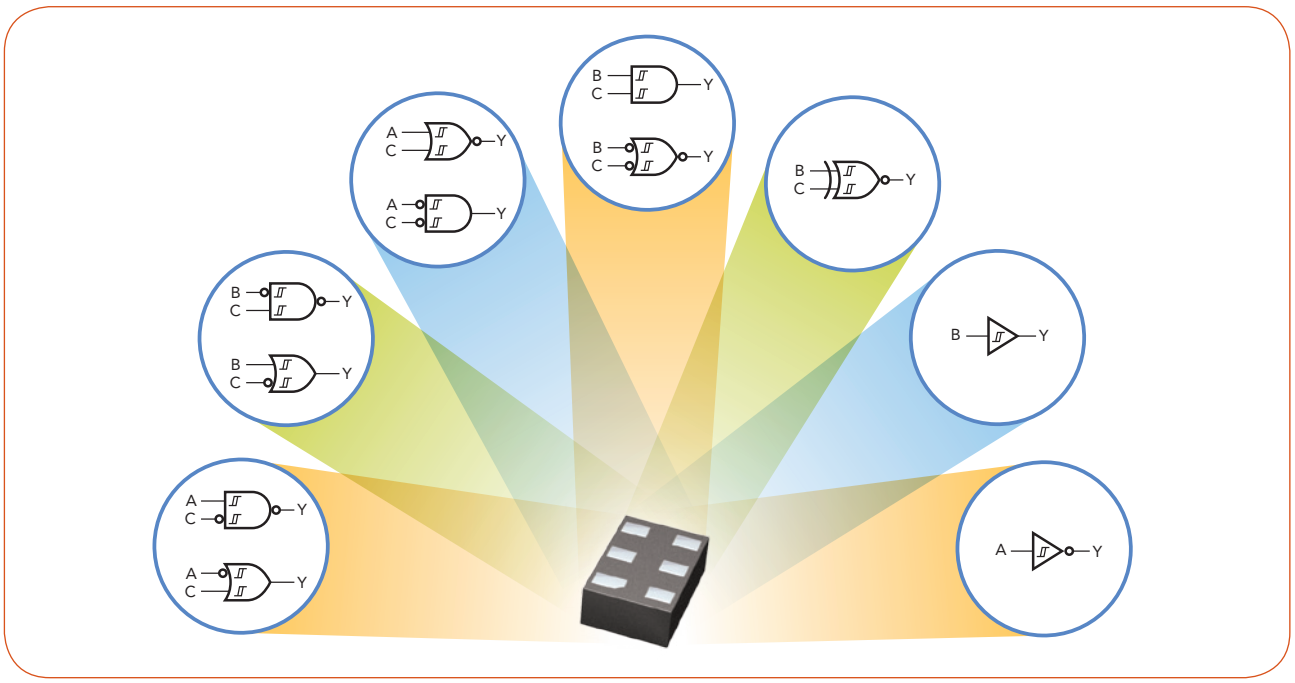
Using a configurable logic device to replace three components in an application (an inverter, a buffer, and an AND gate, for example), means only one device needs to be qualified, not three. Similarly, from a logistics standpoint, the configurable device replaces three types on the BOM, and this reduces inventory costs. In the manufacturing phase, the configurable device requires only one tape-and-reel position in the pick-and-place machine, and this increased efficiency lowers the assembly cost.

Dual PCB configurable logic for more ways to save space and lower cost

Dual PCB configurable logic from NXP combines two configurable logic devices in a single package. It gives engineers a more flexible, more economical way to implement control logic solutions. These advantages can mean lower system cost, improved inventory management, and fewer qualification expenses during development. Simply put, dual PCB configurable logic is the next step in logic design.

Learn more:

www.nxp.com/logic



Configurable logic = one package, nine or more functions


e-mail
From: J.Mich
From: M.Mor
From: S.Joe
From: K.Alek
From: N.Mos
From: S.Bar
atmosphere
green
nature
science
sky
space
sphere
sun
sunlight
symbol

Our approach to quality

At NXP, we recognize the vital importance of quality in electronic components, and understand its critical effect on the viability and economics of finished equipment. This is especially true for semiconductors, which often perform critical circuit functions in harsh environments. Our commitment to quality means we continuously strive to improve our products and processes to ensure they reach the highest possible quality standards.

Zero-defect program

We have an NXP-wide "zero-defect" quality program in place, and view it as a part of our everyday way of doing business. Our pursuit of improvement is ongoing, as we strive to eliminate incidents in production, reduce the rate of incoming complaints, and lower the defect-per-billion (DPB) level to zero.

Six-Sigma program

As part of our overall corporate strategy, we involve the entire organization in process improvement. "Design for Six-Sigma" and "Design for eXcellence" (DfX) are embedded in our processes for creating products. In production, we employ a structured approach to identifying outliers (maverick lots) and defects, and remove them from the manufacturing process to minimize any spill-over effect.

Safe-Launch (DfX)

Our guiding philosophy for all product launches is to achieve a best-in-class DPB level immediately, at the start of production.

Complaint handling

In cooperation with customers, we use continual process improvement to achieve best-in-class performance in handling complaints and solving problems.

Green products

Concern for the environment has driven us to offer a broad portfolio of Dark Green products that are free of lead and halogen, and we comply fully with the European Union's Restriction on Hazardous Substances (RoHS) Directive 2002/95/EC.

Automotive portfolio

To support automotive applications and other applications that operate under extreme conditions, we offer the –Q100 portfolio. These are all qualified to NXP's internal automotive grade, which exceeds the requirements required by the Automotive Electronics Council AEC-Q100 standard.

Certifications and standards

We have achieved certification for all the international standards relevant to our industry, including ISO/IEC 9001, ISO/IEC 14001, and OHSAS 18001, as well as ISO/TS 16949 and VDA 6.3 (for automotive sites).

Portfolio overview

From old favorites to new innovations

We offer one of the broadest selections of logic, from mature BiCMOS families to the latest in advanced, low-power CMOS technology. We constantly find ways to reduce power consumption and minimize footprint. Our advanced CMOS processes deliver robust performance, and are the reason why we can provide so many low-power families that support low-voltage applications.

We are always careful to match the needs of today's applications and systems, and that's why our portfolio focuses on reduced power consumption and smaller size.

We help reduce complexity while adding flexibility, by offering a long list of special features available across a number of families. Also, to support industrial and automotive applications, our logic is available in options that are characterized and specified from -40 to +125 °C.

The NXP logic portfolio includes:

Standard logic functions available in SO, TSSOP and DQFN packages with 14 contacts or more.
Mini Logic functions in smaller footprint PicoGate and MicroPak packages with 10 contacts or less.

Logic portfolio by family, in high- and low-voltage categories

High-voltage families

INCREASING PERFORMANCE

Family	HEF4000B	HC(T)	AHC(T)	VHC(T)	XC7	NPIC	CBT(D)
Supply voltage (V)	3 to 15	2 to 6	2 to 5.5	2 to 5.5	2 to 5.5	2.3 to 5.5	4.5 to 5.5
Propagation delay, typ (ns)	60	9	5	5	5	5	0.25
Output drive (mA)	±3	±8	±8	±8	±8	100	Not applicable
Standby current (µA)	600	80	40	40	40	200	3
Temperature range (°C)	-40 to +85	-40 to +125	-40 to +125	-40 to +125	-40 to +125	-40 to +125	-40 to +85
AEC-Q100 option	•	•	•	•	•	•	•
Process technology							
CMOS	•	•	•	•	•	•	•
Functions							
Gates	•	•	•	•	•		
MSI	•	•	•	•	•	•	
Buffers	•	•					
Analog switches	•	•	•				
Bus interfaces/channels (bits)			8	8			
LED drivers	•					•	
Bus switches							•
Level translators							•
Features							
Overvoltage-tolerant inputs up to 5 V			•	•	•		•
Schmitt-trigger inputs	•	•	•	•	•		
Low-threshold inputs		•	•	•	•		
Open-drain outputs		•	•			•	
Input-clamping diodes	•	•				•	
TTL inputs		•	•	•			•
Low delay isolation							•

Low-voltage families

INCREASING PERFORMANCE

Family	LV	LVC	ALVC	LVT	ALVT	AVC(M)	AUP	AXP	CBTLV(D)
Supply voltage (V)	1 to 3.6[1]	1.2 to 3.6[2]	1.2 to 3.6	2.7 to 3.6	2.3 to 3.6	1.2 to 3.6	0.8 to 3.6	0.7 to 2.75	2.3 to 3.6
Propagation delay, typ (ns)	9	2	2	2	1.5	2	4	3	0.15
Output drive (mA)	±8	±24	±24	-32/64	-32/64	±8	±4	±8	Not applicable
Standby current (µA)	20	20	40	120	90	20	0.9	0.6	10
Temperature range (°C)	-40 to +125	-40 to +125	-40 to +85	-40 to +85	-40 to +125	-40 to +85	-40 to +125	-40 to +85	-40 to +125
AEC-Q100 option	•	•		•		•	•		•
Process technology									
CMOS	•	•	•			•	•	•	•
BiCMOS				•	•				
Functions									
Gates	•	•	•	•			•	•	
MSI	•	•							
Buffers	•	•	•	•	•	•	•	•	
Configurable and combination logic		•					•	•	
Analog switches	•	•							
Bus interfaces/channels (bits)		8/16/32	8/16/32	8/16/32	8/16	16/32			
Bus switches									•
Level translators		•	•			•	•		•
Features									
Bus hold		•	•	•	•	•			
Source termination		•	•	•	•	•			
Live insertion[3]		•		•	•	•	•	•	
Overvoltage-tolerant inputs to 5 V		•		•	•				
Overvoltage-tolerant inputs to 3 V[4]			•			•	•	•	•
Power-off leakage (I_{OFF}) circuitry		•		•	•	•	•	•	
Schmitt-trigger inputs	•	•	•	•	•		•	•	
Low-threshold inputs							•		
Open-drain outputs	•	•					•	•	
Input-clamping diodes	•								
Low delay isolation									•
Rail-to-rail switching									•

[1] Some functions up to 5.5 V
[2] PicoGate functions (1G, 2G, and 3G) operate up to 5.5 V
[3] Functions meet some or all the requirements for live insertion
[4] AXP inputs tolerant to 2.75 V only

Logic portfolio by function

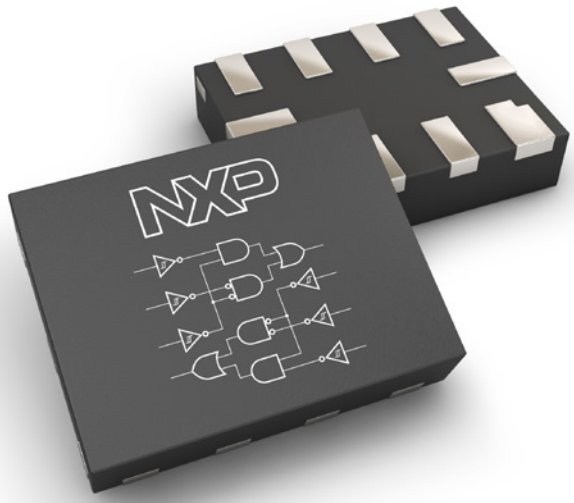
	High-voltage families							Low-voltage families							
Functions	HEF4000B	HC(T)	AHC(T)	VHC(T)	XC7	NPIC	CBT(D)	LV	LVC	ALVC	LVT	ALVT	AVC(M)	AUP	AXP	CBTLV(D)
Analog switches	•	•	•					•	•							
Buffers/inverters/drivers	•	•	•	•	•			•	•	•	•	•	•	•	•	
Bus switches							•									•
Counters/frequency dividers	•	•						•	•							
Decoders/demultiplexers	•	•	•					•	•					•		
Digital comparators	•	•														
Digital multiplexers		•	•					•	•					•		
Encoders		•														
FIFO registers		•														
Flip-flops	•	•	•					•	•	•	•	•	•	•		
Full adders		•														
Gates	•	•	•	•	•			•	•	•	•			•	•	
AND gates	•	•	•	•	•			•	•	•	•			•	•	
Combination gates	•	•							•					•		
Configurable multi-function gates									•					•	•	
EXCLUSIVE-NOR gates	•	•														
EXCLUSIVE-OR gates	•	•	•		•				•					•		
NAND gates	•	•	•					•	•	•	•			•	•	
NOR gates	•	•	•	•	•			•	•	•	•			•	•	
OR gates	•	•	•	•	•			•	•	•	•			•	•	
Latches/registered drivers	•	•	•					•	•	•	•	•	•	•		
Level shifters/translators	•	•							•	•			•	•		
Multivibrators	•	•	•					•	•							
Parity generators/ checkers		•														
Phase-locked loops	•	•														
Schmitt triggers	•	•	•	•	•			•	•	•	•			•	•	
Shift registers/LED drivers	•	•	•	•		•		•	•							
Transceivers		•	•	•				•	•	•	•	•	•			

Special features

NXP offers a variety of special features that improve performance, simplify design, lower cost, reduce the design footprint, and eliminate external components.

This section highlights the features available across a number of families:

The portfolio matrixes on page 14 show the features available in each family.



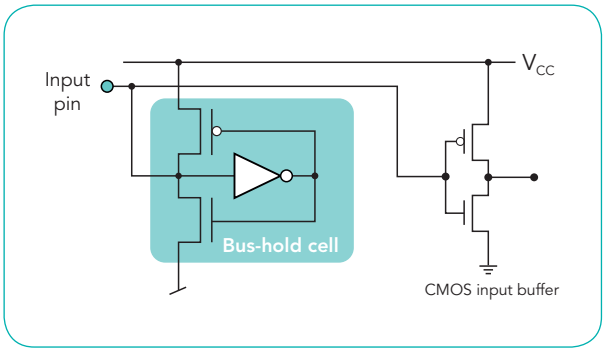
BUS HOLD

What it does

Defines inputs and ensures that oscillations and excessive current consumption, due to floating inputs, are avoided. Can eliminate external pull-up/pull-down resistors.

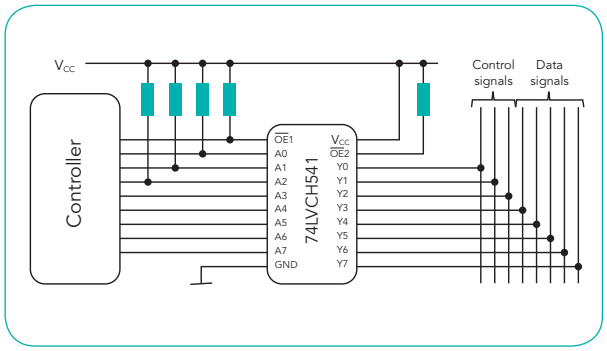
Why it's important

CMOS inputs are high impedance. If they're not defined, they can cause false switching and increase power consumption. The bus-hold feature defines the input by latching in the last logic level applied to the input. This eliminates the external components required to define the inputs, and that saves space, reduces the BOM, and reduces placement cost.



The bus-hold feature

The state of the bus-hold cell is indeterminate at power-up, so external resistors may be needed to set a default state at power-up, as shown here:



Using resistors to set default logic state

Resistors that set the default logic state can be sized as follows:

$R_{PD} < V_{TH}/I_{BHHO}$

$R_{PU} < (V_{CC} - V_{TH})/ I_{BHLO}$

The input switching threshold voltage (V_{TH}) is approximately equal to $(V_{IH} + V_{IL})/2$

Where you'll find it

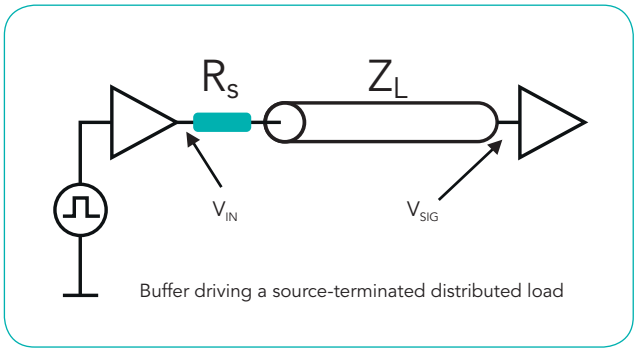
The bus-hold feature is standard on all LVT and ALVT bus-interface products, including 8-, 16-, and 32-bit buffers, inverters, drivers, flip-flops, latches/registered drivers, level shifters/translators, and transceivers. On other families, the bus-hold feature is indicated by an "H" in the product number (e.g. 74LVCH245).

	3.3 V	2.5 V	1.8 V	1.2 V
Bus hold	LVC, ALVC, LVT, ALVT, AVC(M)	LVC, ALVC, ALVT, AVC(M)	LVC, ALVC, AVC(M)	AVC(M)

SOURCE TERMINATION

What it does

Improves impedance matching in distributed systems and eliminates the need for external termination resistors.



Source-termination resistor

Why it's important

Source termination is commonly used to terminate distributed systems so as to avoid issues with signal integrity. The output resistance of the driver is matched to the characteristic impedance of the distributed system using an external resistor. Integrated source termination solves signal-integrity issues associated with distributed systems without the need of external components, and thus reduces BOM and cost.

Where you'll find it

Source-termination options are available in the low-voltage BiCMOS families (LVT and ALVT) and the low-voltage CMOS families [LVC, ALVC, AVC(M)]. Many of NXP's 8-, 16-, and 32-bit products – including buffers, inverters, drivers, flip-flops, latches/registered drivers, and transceivers – have source-termination options. In transceivers, source termination is included on all I/O ports.

A "2" is used to identify device types that include source termination (e.g. 74LVT2244 & 74LVC162244).

	3.3 V	2.5 V	1.8 V	1.2 V
Source-termination resistors	LVC, ALVC, LVT, ALVT, AVC(M)	LVC, ALVC, ALVT, AVC(M)	LVC, ALVC, AVC(M)	AVC(M)

OVERVOLTAGE-TOLERANT INPUTS

What they do

Enable high-to-low voltage-level translation without external components.

Why they're important

Devices with overvoltage-tolerant inputs do not have input clamp diodes on digital inputs, and can be used to interface to higher-voltage systems without using external current-limiting resistors. This reduces BOM and cost.

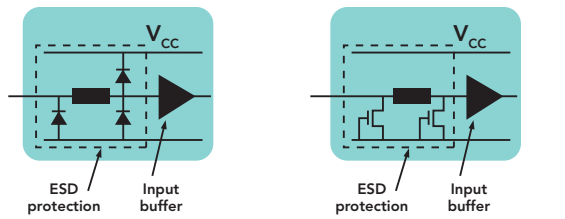
Where you'll find them

The following families, in alphabetical order, have digital inputs that are overvoltage-tolerant and can be used to interface with subsystems operating at a higher supply voltage: AHC, ALVC, ALVT, AUP, AVC, AXP, CBTLV(D), LVC, and LVT. PicoGate devices in the LVC family can be used to interface subsystems with a power supply of 5.0 V to subsystems with a supply of as low as 1.8 V. The table shows the supply range of each family and the maximum input voltage that can be applied.

Family	Input voltage max (V)	Supply voltage (V)
AXP	2.75	0.7 to 2.75
AUP	3.6	0.8 to 3.6
AVC	3.6	1.2 to 3.6
AHC	5.5	2.0 to 5.5
CBTLV(D)	3.6	2.3 to 3.6
LVC	5.5	1.65 to 3.6
LVC PicoGate devices	5.5	1.65 to 5.5
ALVC devices without bus hold	3.6	1.65 to 3.6
LVT	5.5	2.7 to 3.6
ALVT	5.5	2.3 to 3.6

CMOS input with no diode to V_{CC}

The overshoot clamp diode in a typical CMOS input is removed and there is no DC current path to V_{CC} through the inputs. In an input cell with overvoltage protection, as $V_{IN} > V_{CC} + V_t$, no current flows to V_{CC} in the input cell. This feature is available across all voltages. As mentioned above, the AVC and AUP families have a maximum VIN of 3.6 V. The LVC and ALVC families offer the feature on versions without bus hold.



Overvoltage protection provided by CMOS input with no diode to V_{CC}

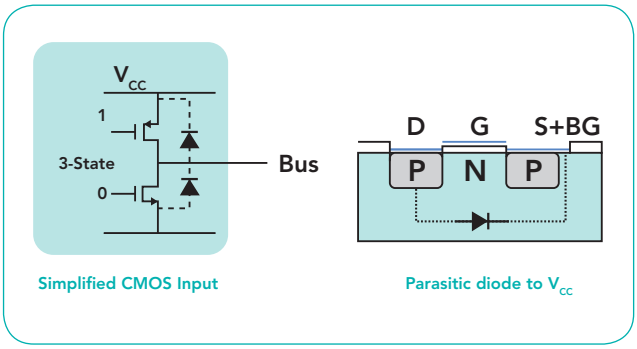
OVERVOLTAGE-TOLERANT OUTPUTS

3-state CMOS output

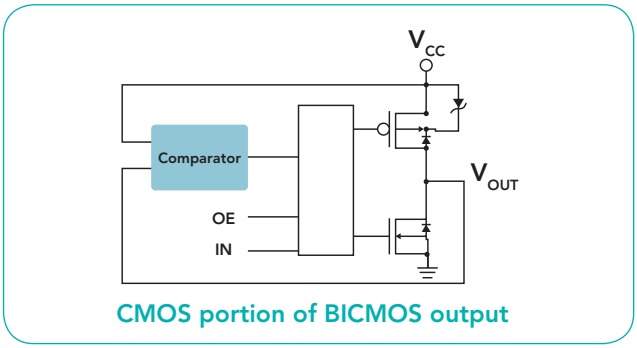
3-stated outputs prevent a current path from the output to the supply voltage when a voltage higher than the supply voltage is applied to the output. In some applications, such as mixed-voltage multi-drop backplane applications, there is a risk of data contention and even damage due to clamping caused by 3-state outputs that are not overvoltage-tolerant. The AUP, AVC(M), AXP, and LVC logic families all have overvoltage-tolerant 3-state CMOS outputs that switch the back gate of the PMOS output driver to V_{CC} or the output voltage, whichever is higher.

3-state BiCMOS output

The LVT and ALVT families have overvoltage-tolerant 3-state BiCMOS outputs. A Schottky diode between V_{CC} and the back gate prevents current flow to V_{CC}. The BiCMOS outputs also include self-protection. The output is set to 3-state when $V_{OUT} > V_{CC} + 0.5$ V.



Overvoltage protection provided by 3-state CMOS output



Overvoltage protection provided by 3-state CMOS output

POWER-OFF LEAKAGE (I_{OFF}) CIRCUITRY

What it does

Prevents potentially damaging leakage paths through the device when it's powered down.

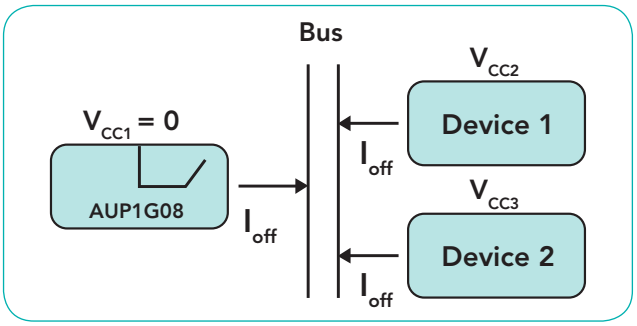
Why it's important

Enables power-management strategies to use partial power-down of subsystems, saves energy in battery-powered applications, and prevents damage to devices in telecommunications-infrastructure applications.

Where you'll find it

The following families, in alphabetical order, include power-off leakage (I_{OFF}) circuitry: ALVC, ALVT, AVC(M), AUP, AXP, LVC, and LVT.

	5 V	3.3 V	2.5 V	1.8 V	1.2 V	0.8 V
Power-off leakage (I_{OFF}) circuitry	LVC	LVC, ALVC, LVT, ALVT, AVC(M), AUP	LVC, ALVC, ALVT, AVC(M), AUP, AXP	LVC, ALVC, AVC(M), AUP, AXP	AVC(M), AUP, AXP	AXP



Disabling power using the I_{OFF} feature

SCHMITT-TRIGGER INPUTS

What it does

Uses input hysteresis to prevent false switching and ensure well-defined outputs when driven by slowly transitioning signals.

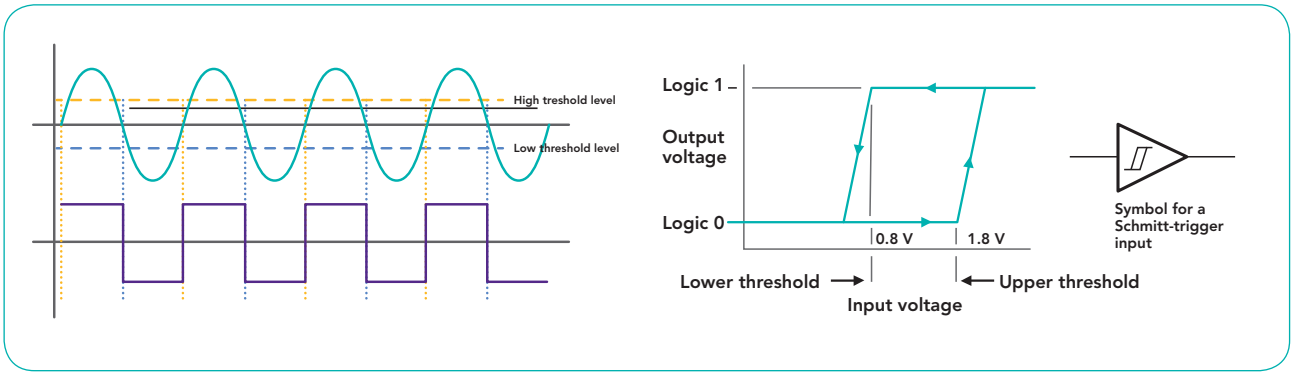
Why it's important

Enables asynchronous analog systems to interface with digital systems.

Where you'll find it

Schmitt-trigger inputs are standard on any of NXP's 14, 17, 132, 4093, 40106, and configurable logic devices.

	5 V	3.3 V	2.5 V	1.8 V	1.2 V	0.8 V
Schmitt-trigger inputs	HEF4000B, HC(T), AHC(T), VHC(T), XC7, LV, LVC	HC, AHC, VHC, XC7, LV, LVC, ALVC, LVT, ALVT, AUP	HC, AHC, VHC, XC7, LVC, ALVC, ALVT	LVC, ALVC, AUP, AXP	AUP, AXP	AXP

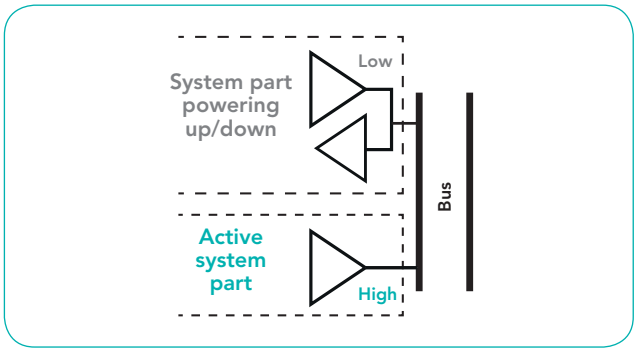


Operation of Schmitt-trigger input

LIVE INSERTION

What it does

Enables the installation or removal of a board while the system is powered up.



Live insertion

Why it's important

Live insertion, which is also known as hot swapping or hot plugging, involves inserting or extracting a board without switching off the power. That minimizes down time, and makes it easier to repair or upgrade a system. The goal is to maintain data integrity on the system bus while preventing damage to components on the host system or on the inserted/extracted card. Various degrees of bus isolation makes this possible.

Where you'll find it

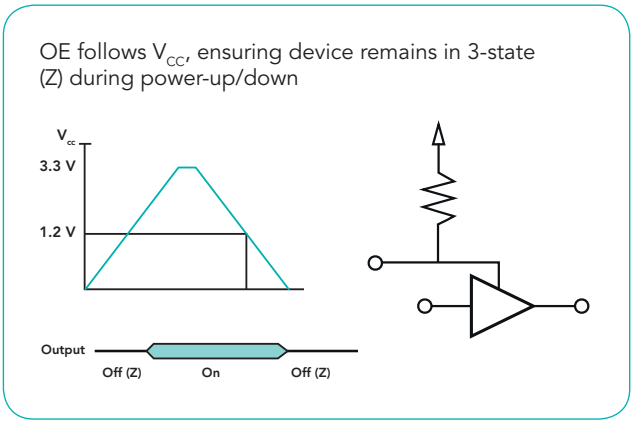
Every NXP logic family supports some level of bus isolation, but live insertion is enabled by using one of three features: I_{OFF} on its own, I_{OFF} with 3-state outputs, or I_{OFF}, 3-state outputs and the BIAS V pin.

Live insertion with I_{OFF}

The I_{OFF} feature, which is described later in this chapter, supports partial power-down mode. Preventing current flow into the inputs and outputs of an unpowered device ensures that, when the device is inserted, the effective load seen on a powered data bus is minimal. Upon detection of the inserted board, the output enable input should be used to prevent data contention on the backplane. Devices that include power-up 3-state allow more time for the inserted board to be detected and the state of the output enable pin to be set.

Live insertion with I_{OFF} and 3-state outputs

This feature, listed in datasheets as I_{PU}/I_{PD} or I_{OZPU}/I_{OZPD}, supports the same power-down mode as I_{OFF}, but adds the ability to keep outputs 3-stated during power-up and power-down. This prevents outputs from turning on before reaching the V_{CC} trip point, as shown in the figure. 3-state power-up mode also prevents the bus from loading at power-up. The 3-state power-up feature is available on NXP's low-voltage LVT and ALVT families (the outputs 3-state below V_{CC} = 1.2 V), and on the 5 V ABT family (the outputs 3-state below V_{CC} = 2 V).



Power-up mode with 3-state outputs

	5 V	3.3 V	2.5 V	1.8 V	1.2 V	0.8 V
Live insertion with I_{OFF}	LVC Mini Logic	LVC, AVC(M), AUP	LVC, ALVC, AVC(M), AUP, AXP	LVC, ALVC, AVC(M), AUP, AXP	AVC(M), AUP, AXP	AXP
Live insertion with I_{OFF} and 3-state outputs		LVT, ALVT				

LOW-THRESHOLD INPUTS

What it does

Support voltage-level translation.

Why it's important

Being able to configure the system to translate voltages, according to the recommended guidelines for the input and output voltage levels of each component, makes the system more predictable, improves overall performance, and saves energy.

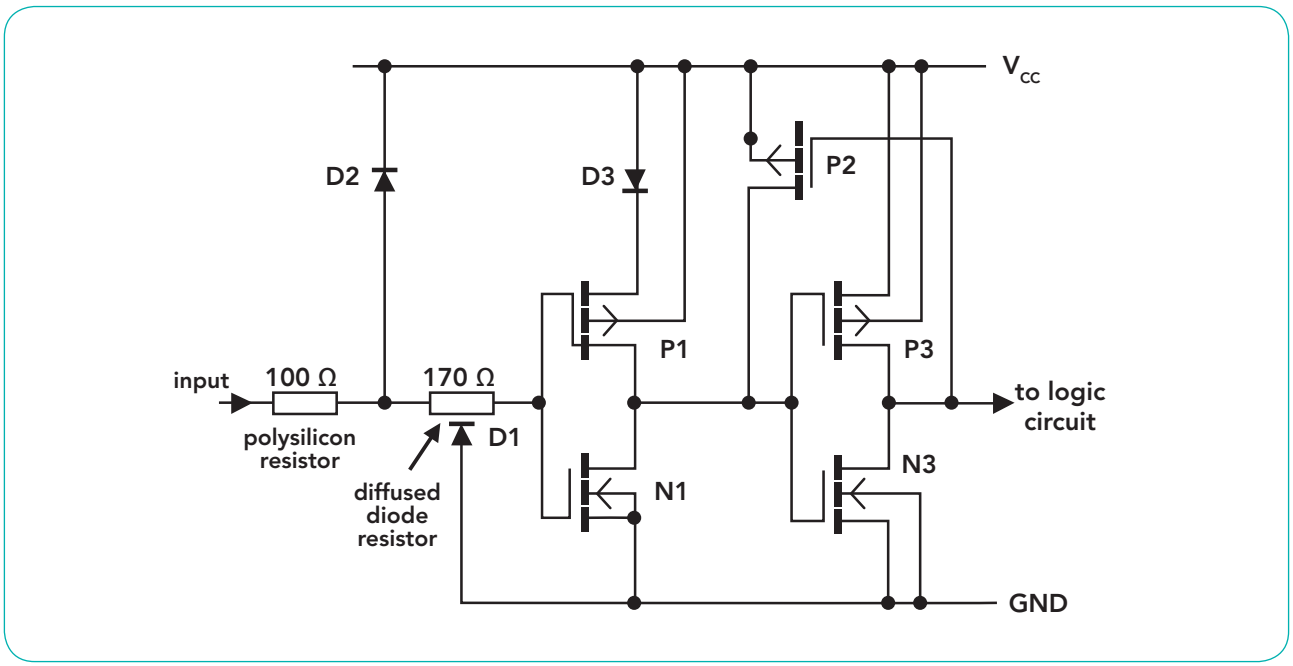
Low-threshold inputs

CMOS devices with input switching thresholds lower than the typical values can be used for low-to-high voltage-level translation.

The circuitry is shown below:

The combination of N1 sizing and drop across D1 determines the input threshold. Also, the P2 PMOS reduces the crossbar current through the inverter. HCT and AHCT products include TTL inputs, they operate at 5 V supply and can be used to interface to 3.3 V outputs. AUP1T devices operate in the 3.6 V range and can be used to interface with 1.8 V outputs.

	5 V	3.3 V	2.5 V	1.8 V
Low-threshold inputs	HCT AHCT VHCT XC7SET	AUP	AUP	AUP

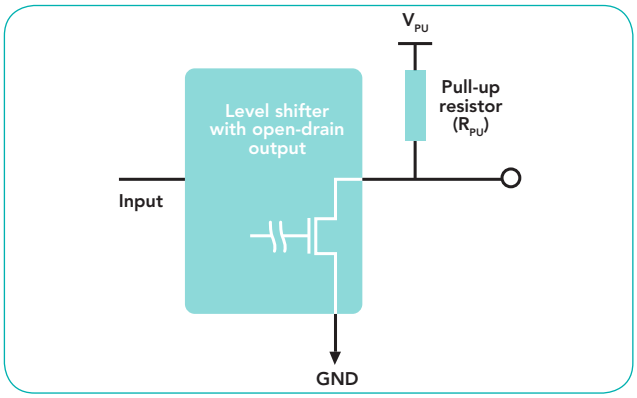


Simplified CMOS input with lower-then-typical threshold values

OPEN-DRAIN OUTPUTS

Open-drain outputs

An open-drain output can be pulled up to a voltage level that matches the requirements of the device it's driving. As shown in the figure, a pull-up resistor (R_{PU}) is used between the output and the pull-up voltage (V_{PU}). V_{PU} can be set higher or lower than V_{CC}, making open-drain outputs suitable for both low-to-high and high-to-low voltage-level translation.



Open-drain output and pull-up resistor for level translation

Where you'll find it

The AHCT and HCT families support legacy TTL levels. They operate at 5 V and can be used to interface with 3.3 V inputs. AUP1T devices operate at 3.3 V and can be used to interface with 1.8 V inputs. The LVT and ALVT families operate at 3.3 V and can be used to interface with 2.5 V inputs. Many of NXP's buffer, inverter, and gate devices include open-drain outputs.

	5 V	3.3 V	2.5 V	1.8 V	1.2 V	0.8 V
Open-drain outputs	HEF4000B, NPIC, HC(T), AHC(T), LV, LVC	HC, AHC, LV, LVC, AUP	LVC, AUP, AXP	AUP, AXP	AUP, AXP	AXP

INPUT-CLAMPING DIODES

What they do

Provide overvoltage and ESD protection, and enable high-to-low level translation.

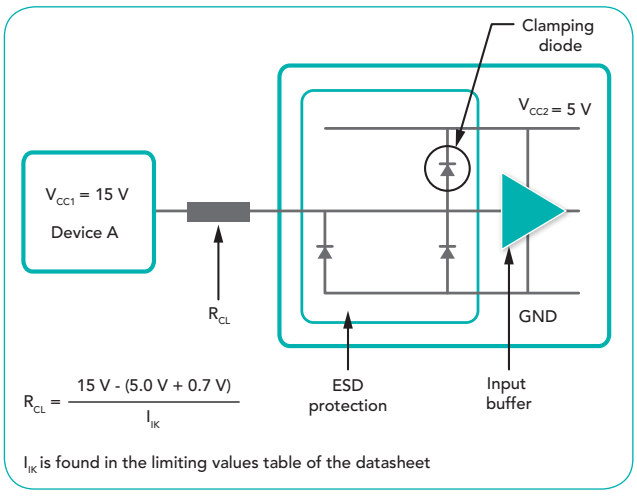
Why they're important

In families that have an input-clamping diode to V_{CC}, the diode is a critical part of the input ESD-protection circuit. The clamping property of the diode can also be used with an external current-limiting resistor so the input can be interfaced to higher voltages. On some NXP logic devices, the inputs have input-clamping diodes to V_{CC} and GND. When using CMOS devices that have current-limiting resistors at the inputs, the input voltage can exceed maximum specified values as long as the maximum current rating is observed.

Where you'll find them

The HEF4000B, HC(T), NPIC, and LV families all utilize ESD-protection circuits that include input-clamping diodes to V_{CC}.

	5 V	3.3 V	2.5 V	1.8 V	1.2 V
Input-clamping diodes	HEF4000B, HC(T), LV	HC, LV	HC, LV	LV	LV



Input-clamping diodes support high-to-low level translation

LOW DELAY ISOLATION

What it does

Enables the isolation of outputs on the same bus line without introducing significant delay.

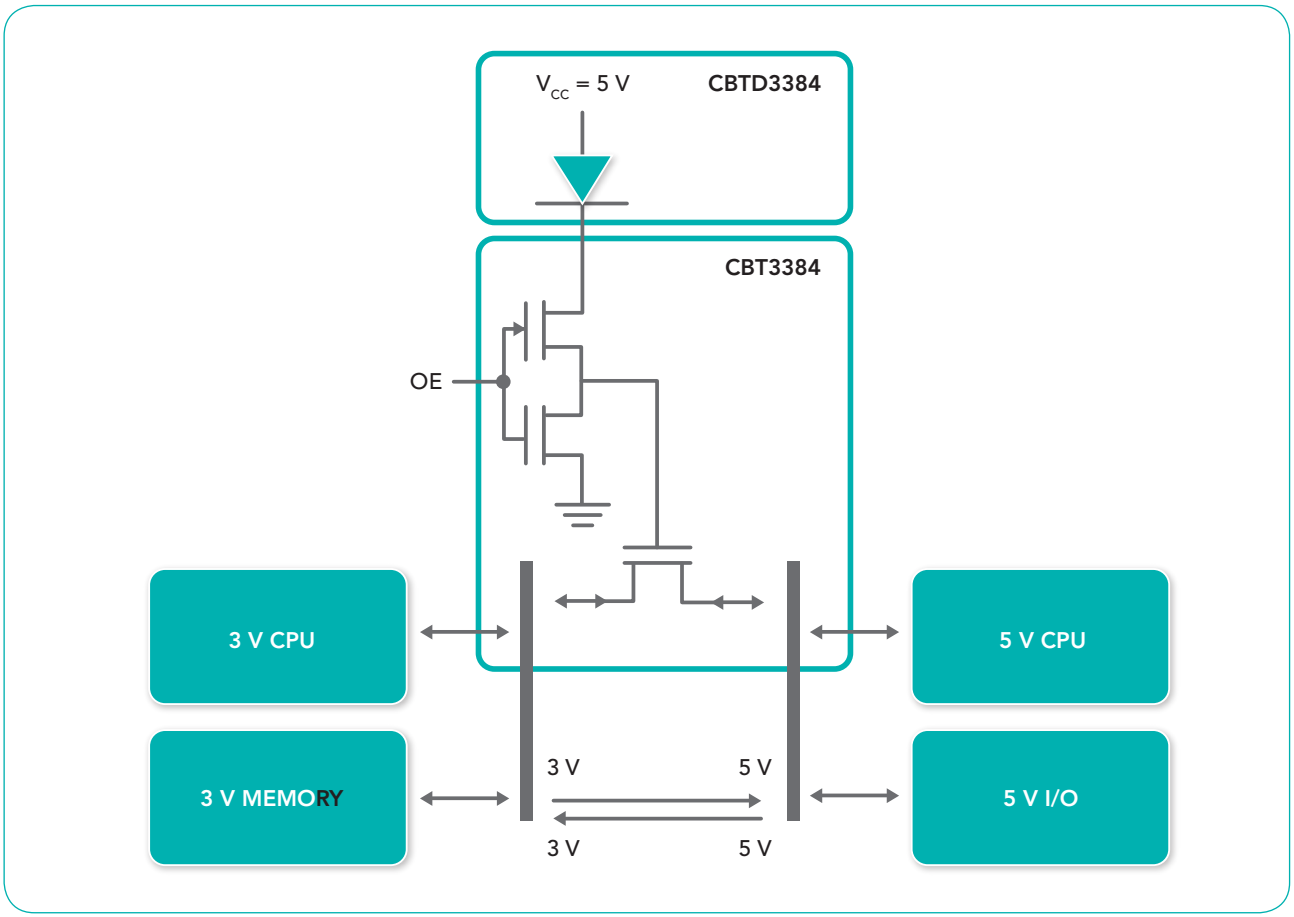
Why it's important

The propagation delay of 3-state buffers used for output isolation can seriously impact the timing margin, and this can be a critical issue in certain designs, including large synchronous backplane applications.

Where you'll find it

NXP's CBT(D) and CBTLV(D) families of bus switches provide isolation with a propagation delay of just 250 ps.

	5 V	3.3 V	2.5 V	1.8 V	1.2 V
Low delay isolation	CBT(D)	CBTLV(D)			



CBT/CBTD3384 switch application

High-voltage families

This section includes the following high-voltage logic families, in ascending order of performance

HEF4000B LOGIC

The HEF4000B series may be one of the oldest CMOS logic families around, but it's still a popular choice due to its ease of design-in, wide operating supply range, excellent noise immunity, and low power consumption.

HEF4000B logic devices are specified over 3 to 15 V and are optimized for 5, 10, and 15 V operation. Equipped with buffered outputs, HEF4000B devices exhibit lower static and dynamic noise than TTL devices. Buffered outputs also result in symmetrical output and improved transfer characteristics as loads increase. HEF4000B logic is pin-compatible with older CMOS4000 and 14500 devices. Due to the LOCMOS process flow, HEF4000B devices offer lower stray capacitances, smaller size, and higher packaging density. Other important features include built-in ESD protection, overvoltage-tolerant inputs, and higher guaranteed fan-out for TTL and LS devices. Standard HEF4000B devices are fully rated from -40 to +85 °C. Packages for extended temperature range (-55 to +125 °C) are available as HEC devices.

Features and benefits

- Supply range from 3 to 15 V
- Standard temperature range of -40 to +85 °C
- Available extended temperature range (HEC) of -55 to +125 °C
- 8/12-bit shift registers can drive 20 mA loads (HEF4x94B)
- Nearly all parts available in TSSOP and SO packages

Applications

- Medical equipment
- General industrial applications
- Consumer electronics
- Toys and games
- Glue-logic applications

HEF4000B selection table

Type number	Function	Description	SO	TSSOP	SSOP
			Suffix T	Suffix TT	Suffix TS
HEF4000B	NOR gates	dual 3-input NOR gate	•		
HEF4001B	NOR gates	quad 2-input NOR gate	•		
HEF4002B	NOR gates	dual 4-input NOR gate	•		
HEF4007UB	Combination	dual complementary pair and inverter	•		
HEF40098B	Buffers/inverters/drivers	hex inverter	•		
HEF40106BP	Schmitt triggers	hex inverter Schmitt trigger	•	•	
HEF40106BTT	Schmitt triggers	hex inverter Schmitt trigger			
HEF4011B	NAND gates	quad 2-input NAND gate	•		
HEF4011UB	NAND gates	quad 2-input NAND gate	•		
HEF4013B	D-type flip-flops	dual D-tye flip-flop with set and reset; positive-edge trigger	•	•	
HEF4014B	Shift registers	8-bit shift register with synchronous parallel enable	•		
HEF4015B	Shift registers	dual 4-bit serial-in/parallel-out shift register	•		
HEF4016B	Analog switches	quad single-pole, single-throw analog switch	•		
HEF40174B	D-type flip-flops	hex D-type flip-flop with reset; positive-edge trigger	•		
HEF40175B	D-type flip-flops	quad D-type flip-flop with reset; positive-edge trigger	•	•	
HEF4017B	BCD/decade counters	Johnson decade counter with 10 decoded outputs	•		
HEF40193B	Binary counters/timers	presettable synchronous 4-bit binary up/down counter; separate up/down clocks	•		
HEF4020B	Binary counters/timers	14-stage binary ripple counter	•		
HEF4021B	Shift registers	8-bit shift register with asynchronous parallel load	•	•	
HEF4023B	NAND gates	triple 3-input NAND gate	•		
HEF40240B	Buffers/inverters/drivers	octal inverter/line driver (3-state)	•		
HEF40244B	Buffers/inverters/drivers	octal buffer/line driver (3-state)	•		
HEF4024B	Binary counters/timers	7-stage binary ripple counter	•		
HEF4025B	NOR gates	triple 3-input NOR gate	•		
HEF4027B	J-K type flip-flops	dual J-K flip-flop	•		
HEF4028B	Decoders/demultiplexers	1-of-10 Decoder	•		
HEF4030B	EXCLUSIVE-OR gates	quad 2-input EXCLUSIVE-OR gate	•		
HEF40373B	Latches/registered drivers	octal D-type transparent latch (3-state)	•		
HEF40374B	D-type flip-flops	octal D-type flip-flop; positive-edge trigger (3-state)	•		
HEF4040B	Binary counters/timers	12-stage binary ripple counter	•		
HEF4043B	Latches/registered drivers	quad R/S latch with set and reset (3-state)	•		
HEF4044B	Latches/registered drivers	quad R/S latch with set and reset (3-state)	•		
HEF4046B	Phase locked loops	phase-locked-loop with VCO	•		
HEF4047B	Multivibrators	monostable/astable multivibrator	•		
HEF4049B	Buffers/inverters/drivers	hex inverter/line driver	•		
HEF4050B	Buffers/inverters/drivers	hex buffer/line driver	•		
HEF4051B	Analog switches	single-pole, octal-throw analog switch	•	•	•
HEF4052B	Analog switches	dual single-pole, quad-throw analog switch	•	•	

HEF4000B selection table (cont.)

Type number	Function	Description	SO	TSSOP	SSOP
			Suffix T	Suffix TT	Suffix TS
HEF4053B	Analog switches	triple single-pole, double-throw analog switch	•	•	
HEF4059B	Divider counters	programmable divide-by-n counter	•		
HEF4060B	Divider counters	14-stage binary ripple counter with oscillator	•		
HEF4066B	Analog switches	quad single-pole, single-throw analog switch	•		
HEF4067B	Analog switches	single-pole, 16-throw analog switch	•		
HEF4068B	NAND gates	8-input NAND gate	•		
HEF4069UB	Buffers/inverters/drivers	hex inverter; unbuffered	•	•	
HEF4070B	EXCLUSIVE-OR gates	quad 2-input EXCLUSIVE-OR gate	•		
HEF4071B	OR gates	quad 2-input OR gate	•		
HEF4072B	OR gates	dual 4-input OR gate	•		
HEF4073B	AND gates	triple 3-input AND gate	•		
HEF4075B	OR gates	triple 3-input OR gate	•		
HEF4077B	EXCLUSIVE-NOR gates	quad 2-input EXCLUSIVE-NOR gate	•		
HEF4081B	AND gates	quad 2-input AND gate	•		
HEF4082B	AND gates	dual 4-input AND gate	•		
HEF4093B	Schmitt triggers	quad 2-input NAND gate Schmitt trigger	•		
HEF4094B	Shift registers	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	•	•	
HEF4104B	Level shifters/ translators	quad low-to-high voltage translator (3-state)	•		
HEF4511B	Decoders/ demultiplexers	BCD to 7-segment latch/decoder/driver with lamp test input	•		
HEF4514B	Decoders/ demultiplexers	4-to-16 decoder/demultiplexer with address latches	•		
HEF4516B	Binary counters/timers	presettable synchronous 4-bit binary up/down counter	•		
HEF4517B	Shift registers	dual 64-bit serial-in/parallel-out shift register	•		
HEF4518B	BCD/decade counters	dual BCD counter	•		
HEF4520B	Binary counters/timers	dual 4-bit synchronous binary counter	•		
HEF4521B	Binary counters/timers	24-stage frequency divider and oscillator	•		
HEF4526B	Binary counters/timers	programmable 4-bit binary down counter	•		
HEF4528B	Multivibrators	dual retriggerable monostable multivibrator with reset	•		
HEF4538B	Multivibrators	dual retriggerable precision monostable multivibrator	•		
HEF4541B	Binary counters/timers	programmable timer	•		
HEF4543B	Decoders/ demultiplexers	BCD to 7-segment latch/decoder/driver with phase input	•		
HEF4555B	Decoders/ demultiplexers	dual 1-to-4 line decoder/demultiplexer	•		
HEF4557B	Shift registers	1-to-64 bit shift register with variable length	•		
HEF4585B	Digital comparators	4-bit magnitude comparator	•		
HEF4794B	Shift registers	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	•		
HEF4894B	Shift registers	12-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	•		

HC(T) LOGIC

HC(T) devices are high-speed CMOS logic available in the industry's broadest range of functions. HC products are for use in CMOS applications from 2.0 to 6.0 V and HCT products are for use in TTL applications from 4.5 to 5.5 V. All HC(T) devices offer a balanced output drive of 8 mA and a typical propagation delay of 9 ns, and are fully specified from -40 to +125 °C.

Features and benefits

- 9 ns typical propagation delay
- Output drive capability I_{OH} / I_{OL} = ±8 mA
- Low power
- Input clamp diodes
- Broad portfolio

Applications

- Industrial
- Consumer electronics
- Computer peripherals

HC(T) selection table

			TSSOP	VSSOP	SSOP	SO	DQFN	MicroPak	PicoGate
Type number	Function	Description	Suffix DP, PW	Suffix DC	Suffix DB	Suffix D	Suffix BQ	Suffix GD, GM, GT	Suffix GW, GV
74HC00	NAND gates	quad 2-input NAND gate	•		•	•	•		
74HCT00	NAND gates	quad 2-input NAND gate; TTL-enabled	•		•	•	•		
74HC02	NOR gates	quad 2-input NOR gate	•		•	•	•		
74HCT02	NOR gates	quad 2-input NOR gate; TTL-enabled	•		•	•	•		
74HC03	NAND gates	quad 2-input NAND gate; open-drain	•		•	•			
74HCT03	NAND gates	quad 2-input NAND gate; open-drain; TTL-enabled	•		•	•			
74HC04	Buffers/inverters/ drivers	hex inverter	•		•	•	•		
74HCT04	Buffers/inverters/ drivers	hex inverter; TTL-enabled	•		•	•	•		
74HC08	AND gates	quad 2-input AND gate	•		•	•	•		
74HCT08	AND gates	quad 2-input AND gate; TTL-enabled	•		•	•	•		
74HC10	NAND gates	triple 3-input NAND gate	•		•	•			
74HCT10	NAND gates	triple 3-input NAND gate; TTL-enabled	•		•	•			
74HC107	J-K type flip-flops	dual J-K flip-flop with reset; negative-edge trigger	•		•	•			
74HCT107	J-K type flip-flops	dual J-K flip-flop with reset; negative-edge trigger; TTL-enabled				•			
74HC109	J-K type flip-flops	dual J-/K flip-flop with set and reset; positive-edge trigger			•	•			
74HCT109	J-K type flip-flops	dual J-/K flip-flop with set and reset; positive-edge trigger; TTL-enabled	•		•	•			
74HC11	AND gates	triple 3-input AND gate	•		•	•			
74HCT11	AND gates	triple 3-input AND gate; TTL-enabled	•		•	•			
74HC112	J-K type flip-flops	dual J-K flip-flop with set and reset; negative-edge trigger	•		•	•			
74HCT112	J-K type flip-flops	dual J-K flip-flop with set and reset; negative-edge trigger; TTL-enabled	•		•	•			
74HC123	Multivibrators	dual retriggerable monostable multivibrator with reset	•		•	•	•		
74HCT123	Multivibrators	dual retriggerable monostable multivibrator with reset; TTL-enabled	•		•	•	•		
74HC125	Buffers/inverters/ drivers	quad buffer/line driver (3-state)	•		•	•	•		

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HCT125	Buffers/inverters/ drivers	quad buffer/line driver (3-state); TTL-enabled	•		•	•			
74HC126	Buffers/inverters/ drivers	quad buffer/line driver (3-state)	•		•	•			
74HCT126	Buffers/inverters/ drivers	quad buffer/line driver (3-state); TTL-enabled	•		•	•			
74HC132	Schmitt triggers	quad 2-input NAND gate Schmitt trigger	•		•	•			
74HCT132	Schmitt triggers	quad 2-input NAND gate Schmitt trigger; TTL-enabled	•		•	•			
74HC138	Decoders/ demultiplexers	3-to-8 line decoder/demultiplexer; inverting	•		•	•	•		
74HCT138	Decoders/ demultiplexers	3-to-8 line decoder/demultiplexer; inverting; TTL-enabled	•		•	•	•		
74HC139	Decoders/ demultiplexers	dual 2-to-4 line decoder/demultiplexer	•		•	•	•		
74HCT139	Decoders/ demultiplexers	dual 2-to-4 line decoder/ demultiplexer; TTL-enabled	•		•	•	•		
74HC14	Schmitt triggers	hex inverter Schmitt trigger	•		•	•	•		
74HCT14	Schmitt triggers	hex inverter Schmitt trigger; TTL-enabled	•		•	•	•		
74HC147	Encoders	10-to-4 line priority encoder			•	•			
74HCT147	Encoders	10-to-4 line priority encoder; TTL-enabled				•			
74HC151	Digital multiplexers	8-input multiplexer	•		•	•			
74HCT151	Digital multiplexers	8-input multiplexer; TTL-enabled	•		•	•			
74HC153	Digital multiplexers	dual 4-input multiplexer	•		•	•			
74HCT153	Digital multiplexers	dual 4-input multiplexer; TTL-enabled	•		•	•			
74HC154	Decoders/ demultiplexers	4-to-16 line decoder/demultiplexer	•		•	•	•		
74HCT154	Decoders/ demultiplexers	4-to-16 line decoder/demultiplexer; TTL-enabled	•		•	•	•		
74HC157	Digital multiplexers	quad 2-input multiplexer	•		•	•	•		
74HCT157	Digital multiplexers	quad 2-input multiplexer; TTL-enabled	•		•	•	•		
74HC160	BCD/decade counters	presettable synchronous BCD decade counter; asynchronous reset	•		•	•			
74HCT160	BCD/decade counters	presettable synchronous BCD decade counter; asynchronous reset; TTL-enabled	•			•			
74HC161	Binary counters/ timers	presettable synchronous 4-bit binary counter; asynchronous reset	•		•	•			
74HCT161	Binary counters/ timers	presettable synchronous 4-bit binary counter; asynchronous reset; TTL-enabled	•		•	•			
74HC163	Binary counters/ timers	presettable synchronous 4-bit binary counter; synchronous reset	•		•	•			
74HCT163	Binary counters/ timers	presettable synchronous 4-bit binary counter; synchronous reset; TTL-enabled	•		•	•			
74HC164	Shift registers	8-bit serial-in/parallel-out shift register	•		•	•	•		
74HCT164	Shift registers	8-bit serial-in/parallel-out shift register; TTL-enabled	•		•	•	•		
74HC165	Shift registers	8-bit parallel or serial-in/serial-out shift register	•		•	•	•		
74HCT165	Shift registers	8-bit parallel or serial-in/serial-out shift register; TTL-enabled	•		•	•	•		

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HC166	Shift registers	8-bit parallel or serial-in/serial-out shift register	•		•	•			
74HCT166	Shift registers	8-bit parallel or serial-in/serial-out shift register; TTL-enabled			•	•			
74HC173	D-type flip-flops	quad D-type flip-flop; positive-edge trigger (3-state)	•		•	•			
74HC174	D-type flip-flops	hex D-type flip-flop with reset; positive-edge trigger	•		•	•			
74HCT174	D-type flip-flops	hex D-type flip-flop with reset; positive-edge trigger; TTL-enabled	•		•	•			
74HC175	D-type flip-flops	quad D-type flip-flop with reset; positive-edge trigger	•		•	•			
74HCT175	D-type flip-flops	quad D-type flip-flop with reset; positive-edge trigger; TTL-enabled	•		•	•			
74HC191	Binary counters/ timers	presettable synchronous 4-bit binary up/down counter	•		•	•			
74HCT191	Binary counters/ timers	presettable synchronous 4-bit binary up/down counter; TTL-enabled				•			
74HC193	Binary counters/ timers	presettable synchronous 4-bit binary up/down counter	•		•	•			
74HCT193	Binary counters/ timers	presettable synchronous 4-bit binary up/down counter; TTL-enabled	•		•	•			
74HC194	Shift registers	4-bit bidirectional parallel or serial-in/ parallel-out shift register			•	•			
74HCT194	Shift registers	4-bit bidirectional parallel or serial-in/ parallel-out shift register; TTL-enabled				•			
74HC1G00	NAND gates	single 2-input NAND gate							•
74HCT1G00	NAND gates	single 2-input NAND gate; TTL-enabled							•
74HC1G02	NOR gates	single 2-input NOR gate							•
74HCT1G02	NOR gates	single 2-input NOR gate; TTL-enabled							•
74HC1G04	Buffers/inverters/ drivers	single inverter							•
74HCT1G04	Buffers/inverters/ drivers	single inverter; TTL-enabled							•
74HC1G08	Buffers/inverters/ drivers	single 2-input AND gate							•
74HCT1G08	AND gates	single 2-input AND gate: TTL-enabled							•
74HC1G125	Buffers/inverters/ drivers	single buffer/line driver (3-state)							•
74HCT1G125	Buffers/inverters/ drivers	single buffer/line driver; TTL-enabled (3-state)							•
74HC1G126	Buffers/inverters/ drivers	single buffer/line driver (3-state)							•
74HCT1G126	Buffers/inverters/ drivers	single buffer/line driver; TTL-enabled (3-state)							•
74HC1G14	Schmitt triggers	single inverter Schmitt trigger;							•
74HCT1G14	Schmitt triggers	single inverter Schmitt trigger; TTL-enabled							•
74HC1G32	OR gates	single 2-input OR gate							•
74HCT1G32	OR gates	single 2-input OR gate; TTL-enabled							•
74HC1G66	Analog switches	single-pole, single-throw analog switch							•
74HCT1G66	Analog switches	single-pole, single-throw analog switch; TTL-enabled							•
74HC1G86	EXCLUSIVE-OR gates	single 2-input EXCLUSIVE-OR gate							•

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HCT1G86	EXCLUSIVE-OR gates	single 2-input EXCLUSIVE-OR gate; TTL-enabled							•
74HC20	NAND gates	dual 4-input NAND gate	•		•	•			
74HCT20	NAND gates	dual 4-input NAND gate; TTL-enabled			•	•			
74HC221	Multivibrators	dual non-retriggerable monostable multivibrator with reset			•	•			
74HCT221	Multivibrators	dual non-retriggerable monostable multivibrator with reset; TTL-enabled			•	•			
74HC238	Decoders/ demultiplexers	3-to-8 decoder/demultiplexer	•		•	•			
74HCT238	Decoders/ demultiplexers	3-to-8 decoder/demultiplexer; TTL-enabled	•		•	•			
74HC240	Buffers/inverters/ drivers	octal inverter/line driver (3-state)	•		•	•			
74HCT240	Buffers/inverters/ drivers	octal inverter/line driver (3-state); TTL-enabled	•		•	•			
74HC241	Buffers/inverters/ drivers	octal buffer/line driver (3-state)	•		•	•			
74HCT241	Buffers/inverters/ drivers	octal buffer/line driver; TTL-enabled (3-state)	•		•	•			
74HC244	Buffers/inverters/ drivers	octal buffer/line driver(3-state)	•		•	•	•		
74HCT244	Buffers/inverters/ drivers	octal buffer/line driver; TTL-enabled (3-state)	•		•	•	•		
74HC245	Transceivers	octal transceiver (3-state)	•		•	•	•		
74HCT245	Transceivers	octal transceiver (3-state); TTL-enabled	•		•	•	•		
74HC251	Digital multiplexers	8-input multiplexer (3-State)	•		•	•			
74HCT251	Digital multiplexers	8-input multiplexer (3-State); TTL-enabled	•		•	•			
74HC253	Digital multiplexers	dual 4-input multiplexer (3-State)			•	•			
74HCT253	Digital multiplexers	dual 4-input multiplexer (3-State); TTL-enabled			•	•			
74HC257	Digital multiplexers	quad 2-input multiplexer (3-State)	•		•	•			
74HCT257	Digital multiplexers	quad 2-input multiplexer (3-State); TTL-enabled	•		•	•			
74HC259	Latches/registered drivers	8 bit addressable latch	•		•	•	•		
74HCT259	Latches/registered drivers	8 bit addressable latch; TTL-enabled	•		•	•	•		
74HC27	NOR gates	triple 3-input NOR gate	•		•	•	•		
74HCT27	NOR gates	triple 3-input NOR gate; TTL-enabled	•		•	•	•		
74HC273	D-type flip-flops	octal D-type flip-flop with reset; positive-edge trigger	•		•	•	•		
74HCT273	D-type flip-flops	octal D-type flip-flop with reset; positive-edge trigger; TTL-enabled	•		•	•	•		
74HC280	Parity generators/ checkers	9-bit odd/even parity generator/ checker				•			
74HCT280	Parity generators/ checkers	9-bit odd/even parity generator/ checker; TTL-enabled			•	•			
74HC299	Shift registers	8-bit universal shift register (3-state)	•		•	•			
74HCT299	Shift registers	8-bit universal shift register (3-state); TTL-enabled	•		•	•			
74HC2G00	NAND gates	dual 2-input NAND gate	•	•				•	
74HCT2G00	NAND gates	dual 2-input NAND gate; TTL-enabled	•	•				•	

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HC2G02	NOR gates	dual 2-input NOR gate	•	•				•	
74HCT2G02	NOR gates	dual 2-input NOR gate; TTL-enabled	•	•				•	
74HC2G04	Buffers/inverters/ drivers	dual inverter							•
74HCT2G04	Buffers/inverters/ drivers	dual inverter; TTL-enabled							•
74HC2G08	AND gates	dual 2-Input AND gate	•	•				•	
74HCT2G08	AND gates	dual 2-Input AND gate; TTL-enabled	•	•				•	
74HC2G125	Buffers/inverters/ drivers	dual buffer/line driver (3-state)	•	•				•	
74HCT2G125	Buffers/inverters/ drivers	dual buffer/line driver (3-state); TTL-enabled	•	•				•	
74HC2G126	Buffers/inverters/ drivers	dual buffer/line driver (3-state)	•	•				•	
74HCT2G126	Buffers/inverters/ drivers	dual buffer/line driver (3-state); TTL-enabled	•	•				•	
74HC2G14	Schmitt triggers	dual inverter Schmitt trigger							•
74HCT2G14	Schmitt triggers	dual inverter Schmitt trigger; TTL-enabled							•
74HC2G17	Schmitt triggers	dual buffer Schmitt trigger							•
74HCT2G17	Schmitt triggers	dual buffer Schmitt trigger; TTL-enabled							•
74HC2G32	OR gates	dual 2-input OR gate	•	•				•	
74HCT2G32	OR gates	dual 2-input OR gate; TTL-enabled	•	•				•	
74HC2G34	Buffers/inverters/ drivers	dual 2-input OR gate							•
74HCT2G34	Buffers/inverters/ drivers	dual buffer; TTL-enabled							•
74HC2G66	Analog switches	dual single-pole, single-throw analog switch	•	•				•	
74HCT2G66	Analog switches	dual single-pole, single-throw analog switch; TTL-enabled	•	•				•	
74HC2G86	EXCLUSIVE-OR gates	dual 2-input EXCLUSIVE-OR gate	•	•				•	
74HCT2G86	EXCLUSIVE-OR gates	dual 2-input EXCLUSIVE-OR gate; TTL-enabled							
74HC30	NAND gates	8-input NAND gate	•		•	•			
74HCT30	NAND gates	8-input NAND gate; TTL-enabled	•		•	•			
74HC32	OR gates	quad 2-input OR gate	•		•	•	•		
74HCT32	OR gates	quad 2-input OR gate; TTL-enabled	•		•	•	•		
74HC365	Buffers/inverters/ drivers	hex buffer/line driver (3-state)	•		•	•			
74HCT365	Buffers/inverters/ drivers	hex buffer/line driver (3-state); TTL-enabled	•		•	•			
74HC366	Buffers/inverters/ drivers	hex buffer/line driver; Inverting (3-state)	•			•			
74HCT366	Buffers/inverters/ drivers	hex inverter/line driver (3-state); Inverting TTL-enabled	•		•	•			
74HC367	Buffers/inverters/ drivers	hex inverter/line driver	•		•	•			
74HCT367	Buffers/inverters/ drivers	hex buffer/line driver (3-state); TTL-enabled	•		•	•			
74HC368	Buffers/inverters/ drivers	hex buffer/line driver; Inverting (3-state)			•	•			

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HCT368	Buffers/inverters/ drivers	hex inverter/line driver; Inverting (3-state); TTL-enabled	•		•	•			
74HC373	Latches/registered drivers	octal D-type transparent latch (3-state)	•		•	•	•		
74HCT373	Latches/registered drivers	octal D-type transparent latch (3-state); TTL-enabled	•		•	•	•		
74HC374	D-type flip-flops	octal D-type flip-flop; positive-edge trigger (3-state)	•		•	•			
74HCT374	D-type flip-flops	octal D-type flip-flop; positive-edge trigger (3-state); TTL-enabled	•		•	•			
74HC377	D-type flip-flops	octal D-type flip-flop with data enable; positive-edge trigger	•		•	•			
74HCT377	D-type flip-flops	octal D-type flip-flop with data enable; positive-edge trigger; TTL-enabled	•		•	•			
74HC390	BCD/decade counters	dual decade ripple counter	•		•	•			
74HCT390	BCD/decade counters	dual decade ripple counter; TTL-enabled	•		•	•			
74HC393	Binary counters/ timers	dual decade ripple counter	•		•	•	•		
74HCT393	Binary counters/ timers	dual 4-bit binary ripple counter; TTL-enabled	•		•	•	•		
74HC3G04	Buffers/inverters/ drivers	triple inverter	•	•				•	
74HCT3G04	Buffers/inverters/ drivers	triple inverter; TTL-enabled	•	•				•	
74HC3G06	Buffers/inverters/ drivers	triple inverter; open-drain	•	•				•	
74HCT3G06	Buffers/inverters/ drivers	triple inverter; open-drain; TTL-enabled	•	•				•	
74HC3G07	Buffers/inverters/ drivers	triple buffer; open-drain	•	•				•	
74HCT3G07	Buffers/inverters/ drivers	triple buffer; open-drain; TTL-enabled	•	•				•	
74HC3G14	Schmitt triggers	triple inverter Schmitt trigger	•	•				•	
74HCT3G14	Schmitt triggers	triple inverter Schmitt trigger; TTL-enabled	•	•				•	
74HC3G34	Buffers/inverters/ drivers	triple buffer	•	•				•	
74HCT3G34	Buffers/inverters/ drivers	triple buffer; TTL-enabled	•	•				•	
74HC4002	NOR gates	dual 4-input NOR gate	•		•	•			
74HCT4002	NOR gates	dual 4-input NOR gate; TTL-enabled			•	•			
74HC40105	FIFO registers	4-bit x 16-word FIFO register	•		•	•			
74HCT40105	FIFO registers	4-bit x 16-word FIFO register; TTL-enabled			•	•			
74HC4015	Shift registers	dual 4-bit serial-in/parallel-out shift register			•	•			
74HCT4015	Shift registers	dual 4-bit serial-in/parallel-out shift register; TTL-enabled				•			
74HC4016	Analog switches	quad single-pole, single-throw analog switch	•			•			
74HCT4016	Analog switches	quad single-pole, single-throw analog switch; TTL-enabled	•						
74HC4017	BCD/decade counters	Johnson decade counter with 10 decoded outputs	•		•	•	•		
74HCT4017	BCD/decade counters	Johnson decade counter with 10 decoded outputs; TTL-enabled				•	•		

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HC4020	Binary counters/ timers	14-stage binary ripple counter	•		•	•	•		
74HCT4020	Binary counters/ timers	14-stage binary ripple counter; TTL-enabled	•		•	•	•		
74HC4040	Binary counters/ timers	12-stage binary ripple counter	•		•	•	•		
74HCT4040	Binary counters/ timers	12-stage binary ripple counter; TTL-enabled	•		•	•	•		
74HC4046A	Phase locked loops	phase-locked-loop with VCO	•		•	•			
74HCT4046A	Phase locked loops	phase-locked-loop with VCO; TTL-enabled			•	•			
74HC4051	Analog switches	single-pole, octal-throw analog switch	•		•	•	•		
74HCT4051	Analog switches	single-pole, octal-throw analog switch; TTL-enabled	•		•	•	•		
74HC4052	Analog switches	dual single-pole, quad-throw analog switch	•		•	•	•		
74HCT4052	Analog switches	dual single-pole, quad-throw analog switch; TTL-enabled	•		•	•	•		
74HC4053	Analog switches	triple single-pole, double-throw analog switch	•		•	•	•		
74HCT4053	Analog switches	triple single-pole, double-throw analog switch; TTL-enabled	•		•	•	•		
74HC4059	Divider counters	programmable divide-by-n counter			•	•			
74HCT4059	Divider counters	programmable divide-by-n counter; TTL-enabled				•			
74HC4060	Binary counters/ timers	14-stage binary ripple counter with oscillator	•		•	•	•		
74HCT4060	Binary counters/ timers	14-stage binary ripple counter with oscillator; TTL-enabled			•	•	•		
74HC4066	Analog switches	quad single-pole, single-throw analog switch	•		•	•	•		
74HCT4066	Analog switches	quad single-pole, single-throw analog switch; TTL-enabled	•		•	•	•		
74HC4067	Analog switches	single-pole, 16-throw analog switch	•		•	•	•		
74HCT4067	Analog switches	single-pole, 16-throw analog switch; TTL-enabled	•		•	•	•		
74HC4075	OR gates	triple 3-input OR gate			•	•			
74HCT4075	OR gates	triple 3-input OR gate; TTL-enabled	•		•	•			
74HC4094	Shift registers	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	•		•	•			
74HCT4094	Shift registers	8-bit serial-in/serial or parallel-out shift register with output register; TTL-enabled (3-state)			•	•			
74HC42	Decoders/ demultiplexers	BCD to decimal decoder (1-of-10)				•			
74HCT42	Decoders/ demultiplexers	BCD to decimal decoder (1-of-10); TTL-enabled				•			
74HC423	Multivibrators	dual retriggerable monostable multivibrator with reset				•	•		
74HCT423	Multivibrators	dual retriggerable monostable multivibrator with reset; TTL-enabled	•		•	•	•		
74HC4316	Analog switches	quad single-pole, single-throw analog switch with translation			•	•	•		
74HCT4316	Analog switches	quad single-pole, single-throw analog switch with translation; TTL-enabled			•	•			
74HC4351	Analog switches	single-pole, octal-throw analog switch with latch	•		•	•			

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HCT4351	Analog switches	single-pole, octal-throw analog switch with latch; TTL-enabled			•	•			
74HCT4353	Analog switches	Triple 2-channel analog multiplexer/ demultiplexer with latch; TTL-enabled				•			
74HC4511	Decoders/ demultiplexers	BCD to 7-segment latch/decoder/ driver with lamp test input				•			
74HCT4511	Decoders/ demultiplexers	BCD to 7-segment latch/decoder/ driver with lamp test input; TTL-enabled				•			
74HC4514	Decoders/ demultiplexers	4-to-16 decoder/demultiplexer with address latches	•		•	•			
74HCT4514	Decoders/ demultiplexers	4-to-16 decoder/demultiplexer with address latches; TTL-enabled	•		•	•			
74HC4515	Decoders/ demultiplexers	4-to-16 decoder/demultiplexer with address latches; inverting				•			
74HCT4515	Decoders/ demultiplexers	4-to-16 decoder/demultiplexer with address latches; inverting; TTL-enabled				•			
74HC4520	Binary counters/ timers	dual 4-bit synchronous binary counter	•		•	•			
74HCT4520	Binary counters/ timers	dual 4-bit synchronous binary counter; TTL-enabled	•		•	•			
74HC4538	Multivibrators	dual retriggerable precision monostable multivibrator	•		•	•			
74HCT4538	Multivibrators	dual retriggerable precision monostable multivibrator; TTL-enabled	•		•	•			
74HC4851	Analog switches	single-pole, octal-throw analog switch	•			•	•		
74HCT4851	Analog switches	single-pole, octal-throw analog switch; TTL-enabled	•			•	•		
74HC4852	Analog switches	dual single-pole, quad-throw analog switch	•			•	•		
74HCT4852	Analog switches	dual single-pole, quad-throw analog switch; TTL-enabled	•			•	•		
74HC540	Buffers/inverters/ drivers	octal inverter/line driver (3-state)			•	•			
74HCT540	Buffers/inverters/ drivers	octal inverter/line driver; TTL-enabled (3-state)			•	•			
74HC541	Buffers/inverters/ drivers	octal buffer/line driver (3-state)	•		•	•			
74HCT541	Buffers/inverters/ drivers	octal buffer/line driver (3-state); TTL-enabled	•		•	•			
74HC5555	Buffers/inverters/ drivers	programmable delay timer with oscillator	•						
74HCT5555	Binary counters/ timers	programmable delay timer with oscillator; TTL-enabled	•						
74HC563	Latches/registered drivers	octal D-type transparent latch; inverting (3-state)	•						
74HCT563	Latches/registered drivers	octal D-type transparent latch; inverting (3-state); TTL-enabled	•		•				
74HC573	Latches/registered drivers	octal D-type transparent latch; inverting (3-state)	•		•	•	•		
74HCT573	Latches/registered drivers	octal D-type transparent latch (3-state); TTL-enabled	•		•	•	•		
74HC574	D-type flip-flops	octal D-type flip-flop; positive-edge trigger (3-state)	•		•	•			
74HCT574	D-type flip-flops	octal D-type flip-flop; positive-edge trigger (3-state); TTL-enabled	•		•	•			
74HC594	Shift registers	8-bit serial-in/parallel-out shift register with output storage register	•		•	•			

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HCT594	Shift registers	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled			•	•			
74HC595	Shift registers	8-bit serial-in/parallel-out shift register with output storage register (3-state)	•		•	•	•		
74HCT595	Shift registers	8-bit serial-in/parallel-out shift register with output storage register (3-state); TTL-enabled	•		•	•	•		
74HC597	Shift registers	8-bit parallel or serial-in/parallel-out shift register with parallel input storage register	•		•	•			
74HCT597	Shift registers	8-bit parallel or serial-in/parallel-out shift register with parallel input storage register; TTL-enabled	•		•	•			
74HC6323A	Binary counters/ timers	programmable ripple counter with oscillator (3-state)				•			
74HC640	Binary counters/ timers	programmable ripple counter with oscillator (3-state)			•	•			
74HCT640	Binary counters/ timers	programmable ripple counter with oscillator (3-state); TTL-enabled			•	•			
74HC652	Transceivers	octal registered transceiver (3-state)	•		•	•			
74HCT652	Transceivers	octal registered transceiver (3-state); TTL-enabled	•			•			
74HC670	Latches/registered drivers	4-bit x 4-word register (3-state)			•	•			
74HCT670	Latches/registered drivers	4-bit x 4-word register (3-state); TTL-enabled			•	•			
74HC688	Digital comparators	8-bit magnitude comparator	•		•	•			
74HCT688	Digital comparators	8-bit magnitude comparator; TTL-enabled	•		•	•			
74HC7030	FIFO registers	9-bit x 64-word FIFO register (3-state)				•			
74HCT7030	FIFO registers	9-bit x 64-word FIFO register (3-state); TTL-enabled				•			
74HCT7046A	Phase locked loops	PLL with lock detector; TTL-enabled				•			
74HC74	D-type flip-flops	dual D-type flip-flop with set and reset; positive-edge trigger	•		•	•	•		
74HCT74	D-type flip-flops	dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	•		•	•	•		
74HC7403	FIFO registers	4-bit x 16-word FIFO register (3-state)				•			
74HCT7403	FIFO registers	4-bit x 16-word FIFO register (3-state); TTL-enabled				•			
74HC7540	Schmitt triggers	octal inverter/line driver Schmitt trigger (3-State)			•	•			
74HCT7540	Schmitt triggers	octal inverter/line driver Schmitt trigger (3-State); TTL-enabled				•			
74HC7541	Schmitt triggers	octal buffer/line driver Schmitt trigger (3-State)	•		•	•			
74HCT7541	Schmitt triggers	octal buffer/line driver Schmitt trigger (3-State); TTL-enabled	•			•			
74HC7731	Shift registers	quad 64-bit shift register	•			•			
74HCT7731	Shift registers	quad 64-bit shift register; TTL-enabled				•			
74HCT85	Digital comparators	4-bit magnitude comparator; TTL-enabled			•	•			
74HC86	EXCLUSIVE-OR gates	quad 2-input EXCLUSIVE-OR gate	•		•	•			
74HCT86	EXCLUSIVE-OR gates	quad 2-input EXCLUSIVE-OR gate; TTL-enabled	•		•	•			

HC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix DP, PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GM, GT	PicoGate Suffix GW, GV
74HC9114	Schmitt triggers	9-bit inverter Schmitt trigger; open-drain (3-state)				•			
74HCT9114	Schmitt triggers	9-bit inverter Schmitt trigger; open-drain (3-state); TTL-enabled				•			
74HC9115	Schmitt triggers	9-bit buffer Schmitt trigger; open-drain (3-state)				•			
74HCT9115	Schmitt triggers	9-bit buffer Schmitt trigger; open-drain (3-state); TTL-enabled				•			
74HC93	Binary counters/ timers	4-bit binary ripple counter			•	•			
74HCT93	Binary counters/ timers	4-bit binary ripple counter; TTL-enabled				•			
74HC05	Buffers/inverters/ drivers	hex inverter; open-drain	•			•	•		
74HC137	Decoders/ demultiplexers	3-to-8 line decoder/demultiplexer with address latches; inverting	•		•	•			
74HC158	Digital multiplexers	quad 2-input multiplexer; inverting				•			
74HC1GU04	Buffers/inverters/ drivers	single inverter; unbuffered							•
74HC21	AND gates	dual 4-input AND gate	•		•	•			
74HC237	Decoders/ demultiplexers	3-to-8 decoder/demultiplexer with address latches	•		•	•			
74HC243	Transceivers	quad transceiver (3-state)			•	•			
74HC283	Full adders	4-bit binary full adder with fast carry	•		•	•			
74HC2GU04	Buffers/inverters/ drivers	Dual inverter; unbuffered							•
74HC3GU04	Buffers/inverters/ drivers	Triple inverter; unbuffered	•	•				•	
74HC40103	Binary counters/ timers	8-bit synchronous binary down counter	•		•	•			
74HC4024	Binary counters/ timers	7-stage binary ripple counter	•		•	•			
74HC4049	Level shifters/ translators	hex inverter with 15V tolerant inputs	•		•	•			
74HC4050	Level shifters/ translators	hex inverter with 15V tolerant inputs	•		•	•			
74HC564	D-type flip-flops	octal D-type flip-flop; inverting; positive-edge trigger (3-state)	•			•			
74HC58	Combination	dual AND-OR gate			•	•			
74HC590	Binary counters/ timers	8-bit binary counter with output register (3-state)	•			•	•		
74HC7014	Schmitt triggers	hex buffer precision Schmitt trigger	•			•			
74HC7266	EXCLUSIVE-NOR gates	quad 2-input EXCLUSIVE-NOR gate			•	•			
74HC73	J-K type flip-flops	dual J-K flip-flop with reset; negative-edge trigger	•		•	•			
74HC75	Latches/registered drivers	Quad Bistable Transparent Latch	•		•	•			
74HCT534N	D-type flip-flops	octal D-type flip-flop; inverting; positive-edge trigger; TTL-enabled (3-state)				•			
74HCT7273	D-type flip-flops	octal D-type flip-flop; inverting; positive-edge trigger; TTL-enabled (3-state)				•			
74HCT9046A	Phase locked loops	PLL with bandgap controlled VCO; TTL-enabled	•			•			
74HCU04	Buffers/inverters/ drivers	hex inverter; unbuffered	•		•	•	•		

AHC(T) LOGIC

AHC(T) devices are advanced high-speed CMOS logic. They are upgrades of the HC(T) family, with overvoltage-tolerant inputs for true mixed-voltage applications. AHC devices are for use in CMOS applications from 2.0 to 6.0 V and AHCT devices are for use in TTL applications from 4.5 to 5.5 V. All AHC(T) devices offer a balanced output drive of 8 mA and a typical propagation delay of 5 ns, and are fully specified from -40 to +125 °C.

Features and benefits

- Typical propagation delay of 5 ns
- Output drive capability I_{OH} / I_{OL} = ±8 mA
- Low power
- 5 V tolerant inputs
- Low noise: V_{OLP} = 0.8 V (max.)

Applications

- Industrial
- Consumer electronics
- Computer peripherals
- Communications

AHC(T) selection table (cont.)

			TSSOP	VSSOP	SSOP	SO	DQFN	MicroPak	PicoGate
Type number	Function	Description	Suffix PW	Suffix DC	Suffix DB	Suffix D	Suffix BQ	Suffix GD, GF, GM, GN, GS, GT	Suffix DP, GW, GV
74AHC00	NAND gate	Quad 2-input NAND gate	•			•	•		
74AHCT00	NAND gate	Quad 2-input NAND gate; TTL-enabled	•			•	•		
74AHC02	NOR gate	Quad 2-input NOR gate	•			•	•		
74AHCT02	NOR gate	Quad 2-input NOR gate; TTL-enabled	•			•	•		
74AHC04	Buffer/inverter/ driver	Hex inverter	•			•	•		
74AHCT04	Buffer/inverter/ driver	Hex inverter; TTL-enabled	•			•	•		
74AHC08	AND gate	Quad 2-input AND gate	•			•	•		
74AHCT08	AND gate	Quad 2-input AND gate; TTL-enabled	•			•	•		
74AHC123A	Multivibrator	Dual retriggerable monostable multivibrator with reset	•			•	•		
74AHCT123A	Multivibrator	Dual retriggerable monostable multivibrator with reset; TTL-enabled	•			•	•		
74AHC125	Buffer/inverter/ driver	Quad buffer/line driver (3-state)	•			•	•		
74AHCT125	Buffer/inverter/ driver	Quad buffer/line driver; TTL-enabled (3-state)	•			•	•		
74AHC126	Buffer/inverter/ driver	Quad buffer/line driver (3-state)	•			•	•		
74AHCT126	Buffer/inverter/ driver	Quad buffer/line driver; TTL-enabled (3-state)	•			•	•		
74AHC132	Schmitt trigger	Quad 2-input NAND gate Schmitt trigger	•			•	•		
74AHCT132	Schmitt trigger	Quad 2-input NAND gate Schmitt trigger; TTL-enabled	•			•	•		
74AHC138	Decoder/ demultiplexer	3-to-8 line decoder/demultiplexer; inverting	•			•	•		
74AHCT138	Decoder/ demultiplexer	3-to-8 line decoder/demultiplexer; inverting; TTL-enabled	•			•	•		
74AHC139	Decoder/ demultiplexer	Dual 2-to-4 line decoder/ demultiplexer	•			•			
74AHCT139	Decoder/ demultiplexer	Dual 2-to-4 line decoder/ demultiplexer; TTL-enabled	•			•			
74AHC14	Schmitt trigger	Hex inverter Schmitt trigger	•			•	•		

AHC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GF, GM, GN, GS, GT	PicoGate Suffix DP, GW, GV
74AHCT14	Schmitt trigger	Hex inverter Schmitt trigger; TTL-enabled	•			•	•		
74AHC157	Digital multiplexer	Quad 2-input multiplexer	•			•	•		
74AHCT157	Digital multiplexer	Quad 2-input multiplexer; TTL-enabled	•			•	•		
74AHC164	Shift register	8-bit serial-in/parallel-out shift register	•			•	•		
74AHCT164	Shift register	8-bit serial-in/parallel-out shift register; TTL-enabled	•			•	•		
74AHC1G00	NAND gate	Single 2-input NAND gate							•
74AHCT1G00	NAND gate	Single 2-input NAND gate; TTL-enabled							•
74AHC1G02	NOR gate	Single 2-input NOR gate							•
74AHCT1G02	NOR gate	Single 2-input NOR gate; TTL-enabled							•
74AHC1G04	Buffer/inverter/ driver	Single inverter							•
74AHCT1G04	Buffer/inverter/ driver	Single inverter; TTL-enabled							•
74AHC1G06	Buffer/inverter/ driver	Single inverter; open drain							•
74AHCT1G06	Buffer/inverter/ driver	Single inverter; open drain; TTL-enabled							•
74AHC1G07	Buffer/inverter/ driver	Single buffer; open drain							•
74AHCT1G07	Buffer/inverter/ driver	Single buffer; open drain; TTL-enabled							•
74AHC1G08	AND gate	Single 2-input AND gate							•
74AHCT1G08	AND gate	Single 2-input AND gate; TTL-enabled							•
74AHC1G125	Buffer/inverter/ driver	Single buffer/line driver (3-state)						•	
74AHCT1G125	Buffer/inverter/ driver	Single buffer/line driver; TTL-enabled (3-state)						•	
74AHC1G126	Buffer/inverter/ driver	Single buffer/line driver (3-state)						•	
74AHCT1G126	Buffer/inverter/ driver	Single buffer/line driver; TTL-enabled (3-state)						•	
74AHC1G14	Schmitt trigger	Single inverter Schmitt trigger							•
74AHCT1G14	Schmitt trigger	Single inverter Schmitt trigger; TTL-enabled							•
74AHC1G17	Schmitt trigger	Single buffer with Schmitt trigger						•	
74AHCT1G17	Schmitt trigger	Single buffer with Schmitt trigger; TTL-enabled						•	
74AHC1G32	OR gate	Single 2-input OR gate							•
74AHCT1G32	OR gate	Single 2-input OR gate							•
74AHC1G66	Analog switch	Single-pole, Single-throw analog switch							•
74AHCT1G66	Analog switch	Single-pole, Single-throw analog switch; TTL-enabled							•
74AHC1G79	D-type flip-flop	Single D-type flip-flop; positive-edge trigger							•
74AHCT1G79	D-type flip-flop	Single D-type flip-flop; positive-edge trigger; TTL-enabled							•
74AHC1G86	EXCLUSIVE-OR gate	2-input EXCLUSIVE-OR gate							•

AHC(T) selection table (cont.)

Type number	Function	Description	TSSOP Suffix PW	VSSOP Suffix DC	SSOP Suffix DB	SO Suffix D	DQFN Suffix BQ	MicroPak Suffix GD, GF, GM, GN, GS, GT	PicoGate Suffix DP, GW, GV
74AHCT1G86	EXCLUSIVE-OR gate	2-input EXCLUSIVE-OR gate TTL-enabled							•
74AHC240	Buffer/inverter/driver	Octal inverter/line driver (3-state)					•		
74AHCT240	Buffer/inverter/driver	Octal inverter/line driver; TTL-enabled (3-state)	•			•	•		
74AHC244	Buffer/inverter/driver	Octal buffer/line driver (3-state)	•			•	•		
74AHCT244	Buffer/inverter/driver	Octal buffer/line driver; TTL-enabled (3-state)	•			•	•		
74AHC245	Transceiver	Octal transceiver (3-state)	•			•	•		
74AHCT245	Transceiver	Octal transceiver; TTL-enabled (3-state)	•			•	•		
74AHC257	Digital multiplexer	Quad 2-input multiplexer (3-state)	•			•			
74AHCT257	Digital multiplexer	Quad 2-input multiplexer; TTL-enabled (3-state)	•			•			
74AHC259	Latch/registered driver	8 bit addressable latch	•			•			
74AHCT259	Latch/registered driver	8-Bit addressable latch; TTL-enabled	•			•			
74AHC273	D-type flip-flop	Octal D-type flip-flop with reset; positive-edge trigger	•			•	•		
74AHCT273	D-type flip-flop	Octal D-type flip-flop with reset; positive-edge trigger; TTL-enabled	•			•	•		
74AHC2G00	NAND gate	Dual 2-input NAND gate		•				•	•
74AHCT2G00	NAND gate	Dual 2-input NAND gate; TTL-enabled		•				•	•
74AHC2G08	AND gate	Dual 2-input AND gate		•				•	•
74AHCT2G08	AND gate	Dual 2-Input AND gate; TTL-enabled		•				•	•
74AHC2G125	Buffer/inverter/driver	Dual buffer/line driver (3-state)		•				•	•
74AHCT2G125	Buffer/inverter/driver	Dual buffer/line driver; TTL-enabled (3-state)		•				•	•
74AHC2G126	Buffer/inverter/driver	Dual buffer/line driver (3-state)		•				•	•
74AHCT2G126	Buffer/inverter/driver	Dual buffer/line driver; TTL-enabled (3-state)		•				•	•
74AHC2G241	Buffer/inverter/driver	Dual buffer/line driver (3-state)		•				•	•
74AHCT2G241	Buffer/inverter/driver	Dual buffer/line driver; TTL-enabled (3-state)		•				•	•
74AHC2G32	OR gate	Dual 2-input OR gate		•				•	•
74AHCT2G32	OR gate	Dual 2-input OR gate		•				•	•
74AHC30	NAND gate	8-input NAND gate	•			•	•		
74AHCT30	NAND gate	8-input NAND gate; TTL-enabled	•			•	•		
74AHC32	OR gate	Quad 2-input OR gate	•			•	•		
74AHCT32	OR gate	Quad 2-input OR gate; TTL-enabled	•			•	•		
74AHC373	Latch/registered driver	Octal D-type transparent latch (3-state)	•			•			
74AHCT373	Latch/registered driver	Octal D-type transparent latch; TTL-enabled (3-state)	•			•			

AHC(T) selection table (cont.)

Type number	Function	Description	TSSOP	VSSOP	SSOP	SO	DQFN	MicroPak	PicoGate
			Suffix PW	Suffix DC	Suffix DB	Suffix D	Suffix BQ	Suffix GD, GF, GM, GN, GS, GT	Suffix DP, GW, GV
74AHC374	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•			•			
74AHCT374	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•			•			
74AHC377	D-type flip-flop	Octal D-type flip-flop with data enable; positive-edge trigger	•			•			
74AHCT377	D-type flip-flop	Octal D-type flip-flop with data enable; positive-edge trigger; TTL-enabled	•			•			
74AHC3G04	Buffer/inverter/ driver	Triple inverter		•				•	•
74AHCT3G04	Buffer/inverter/ driver	Triple inverter; TTL-enabled		•				•	•
74AHC3G14	Schmitt trigger	Triple inverter Schmitt trigger		•				•	•
74AHCT3G14	Schmitt trigger	Triple inverter Schmitt trigger; TTL-enabled		•				•	•
74AHC541	Buffer/inverter/ driver	Octal buffer/line driver (3-state)	•			•	•		
74AHCT541	Buffer/inverter/ driver	Octal buffer/line driver; TTL-enabled (3-state)	•			•	•		
74AHC573	Latch/ registered driver	Octal D-type transparent latch (3-state)	•			•	•		
74AHCT573	Latch/ registered driver	Octal D-type transparent latch; TTL-enabled (3-state)	•			•	•		
74AHC574	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•			•	•		
74AHCT574	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger; TTL-enabled (3-state)	•			•	•		
74AHC594	Shift register	8-bit serial-in/parallel-out shift register with output storage register	•		•	•	•		
74AHCT594	Shift register	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled	•		•	•	•		
74AHC595	Shift register	8-bit serial-in/parallel-out shift register with output storage register (3-state)	•			•	•		
74AHCT595	Shift register	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	•			•	•		
74AHC74	D-type flip-flop	Dual D-type flip-flop with set and reset; positive-edge trigger	•			•	•		
74AHCT74	D-type flip-flop	Dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	•			•	•		
74AHC86	EXCLUSIVE-OR gate	Quad 2-input EXCLUSIVE-OR gate	•			•	•		
74AHCT86	EXCLUSIVE-OR gate	Quad 2-input EXCLUSIVE-OR gate; TTL-enabled	•			•	•		
74AHC1G09	AND gate	Single 2-input AND gate; open drain							•
74AHC1GU04	Buffer/inverter/ driver	Single inverter; unbuffered							•
74AHC3GU04	Buffer/inverter/ driver	Triple inverter; unbuffered		•				•	•
74AHCU04	Buffer/inverter/ driver	Hex inverter; unbuffered	•			•	•		

VHC(T) LOGIC

VHC and VHCT devices are high-speed CMOS logic. They are upgrades of the HC(T) family, with overvoltage-tolerant inputs for true mixed-voltage applications. VHC products are for use in CMOS applications from 2.0 to 6.0 V. VHCT products are for use in TTL applications from 4.5 to 5.5 V. All VHC(T) devices offer balanced output drive of 8 mA and a typical propagation delay of 5 ns, and are fully specified from -40 to +125 °C.

Features and benefits

- Typical propagation delay of 5 ns
- Balanced output drive I_{OH} / I_{OL} = ±8 mA
- Low power
- 5 V tolerant inputs
- Low noise: V_{OLP} = 0.8 V (max.)

Applications

- Industrial
- Consumer electronics
- Computer peripherals
- Communications
- Mixed-voltage applications

VHC(T) selection table

			TSSOP	SO	QFN
Type number	**Function**	**Description**	**Suffix PW**	**Suffix D**	**Suffix BQ**
74VHC02	NOR gates	quad 2-input NOR gate	•	•	•
74VHCT02	NOR gates	quad 2-input NOR gate; TTL-enabled	•	•	•
74VHC08	AND gates	quad 2-input AND gate	•	•	•
74VHCT08	AND gates	quad 2-input AND gate; TTL-enabled	•	•	•
74VHC125	Buffers/inverters/drivers	quad buffer/line driver (3-state)	•	•	•
74VHCT125	Buffers/inverters/drivers	quad buffer/line driver (3-state)	•	•	•
74VHC126	Buffers/inverters/drivers	quad buffer/line driver (3-state)	•	•	•
74VHCT126	Buffers/inverters/drivers	quad buffer/line driver (3-state); TTL-enabled	•	•	•
74VHC14	Schmitt triggers	hex inverter Schmitt trigger	•	•	•
74VHCT14	Schmitt triggers	hex inverter Schmitt trigger; TTL-enabled	•	•	•
74VHC244	Buffers/inverters/drivers	octal inverter/line driver (3-state)	•	•	•
74VHCT244	Buffers/inverters/drivers	octal inverter/line driver (3-state); TTL-enabled	•	•	•
74VHC245	Transceivers	octal transceiver (3-state)	•	•	•
74VHCT245	Transceivers	octal transceiver; TTL-enabled (3-state)	•	•	•
74VHC32	OR gates	quad 2-input OR gate	•	•	•
74VHCT32	OR gates	quad 2-input OR gate; TTL-enabled	•	•	•
74VHC541	Buffers/inverters/drivers	octal buffer/line driver (3-state)	•	•	•
74VHCT541	Buffers/inverters/drivers	octal buffer/line driver (3-state); TTL-enabled	•	•	•
74VHC595	Shift registers	8-bit serial-in/parallel-out shift register with output storage register (3-state)	•	•	•
74VHCT595	Shift registers	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	•	•	•

XC7 LOGIC

XC7 devices are very high-speed CMOS logic. They are upgrades of the HC(T) family, with overvoltage-tolerant inputs for true mixed-voltage applications. XC7SH and XC7WH products are for use in CMOS applications that range from 2.0 to 6.0 V. XC7SET products are for use in TTL applications from 4.5 to 5.5 V. All XC7 devices offer a balanced output drive of 8 mA and a typical propagation delay of 5 ns, and are fully specified from -40 to +125 °C.

Features and benefits

- Typical propagation delay of 5 ns
- Balanced output drive I_{OH} / I_{OL} = ±8 mA
- Low power
- 5 V tolerant inputs
- Low noise: V_{OLP} = 0.8 V (max.)

Applications

- Industrial
- Consumer electronics
- Computer peripherals
- Communications
- Mixed-voltage applications

XC7 selection table

			MicroPak	PicoGate	VSSOP
Type number	Function	Description	Suffix GD, GM, GF, GT	Suffix DP, GW, GV	Suffix DC
XC7SET02	NOR gates	single 2-input NOR gate; TTL-enabled		•	
XC7SET04	Buffers/inverters/drivers	single inverter; TTL-enabled		•	
XC7SET08	AND gates	single 2-input AND gate; TTL-enabled		•	
XC7SET125	Buffers/inverters/drivers	single buffer/line driver; TTL-enabled (3-state)	•	•	
XC7SET14	Schmitt triggers	single inverter Schmitt trigger; TTL-enabled		•	
XC7SET32	OR gates	single 2-input OR gate; TTL-enabled		•	
XC7SET86	EXCLUSIVE-OR gates	2-input EXCLUSIVE-OR gate; TTL-enabled		•	
XC7SH02	NOR gates	single 2-input NOR gate		•	
XC7SH04	Buffers/inverters/drivers	single inverter		•	
XC7SH08	AND gates	single 2-input AND gate		•	
XC7SH125	Buffers/inverters/drivers	single buffer/line driver (3-state)	•	•	
XC7SH14	Schmitt triggers	single inverter Schmitt trigger		•	
XC7SH32	OR gates	single 2-input OR gate		•	
XC7SH86	EXCLUSIVE-OR gates	2-input EXCLUSIVE-OR gate		•	
XC7SHU04	Buffers/inverters/drivers	single inverter; unbuffered		•	
XC7WH126	Buffers/inverters/drivers	dual buffer/line driver (3-state)		•	•
XC7WH14	Schmitt triggers	triple inverter Schmitt trigger	•	•	•
XC7WT14	Schmitt triggers	triple inverter Schmitt trigger	•	•	•

NPIC LOGIC

The NPIC family is a series of LED drivers based on shift registers. When used for I/O expansion, they enable the use of a low-cost controller with a low pincount. The serial output supports cascading, making it possible for three controller I/O to control the state of 16, 24, or more LEDs. They are fully specified from -40 to +125 °C.

Features and benefits

- 33 V, 100 mA open-drain outputs
- Simple 3.3 or 5 V control interface
- I/O expansion
- High frequency
- Cascadable

Applications

- LED drivers
- Displays
- Control units

NPIC selection table

			TSSOP	SO	DQFN
Type number	Function	Description	Suffix PW	Suffix D	Suffix BQ
NPIC6C4894	Shift register	12-bit serial-in/parallel-out shift register with output storage register (3-state)	•	•	
NPIC6C595	Shift register	8-bit serial-in/parallel-out shift register with output storage register (3-state)	•	•	•
NPIC6C596	Shift register/LED driver	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	•	•	•
NPIC6C596A	Shift register/LED driver	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	•	•	•

CBT(D) LOGIC

CBT and CBTD bus switches are low-delay, single-transistor or transmission-gate solutions for multiplexing data buses, hot-swapping boards in backplanes, memory interleaving, signal conditioning, or unidirectional level shifting. They are fully specified from either -40 to +85 °C or from -40 to +125 °C.

Features and benefits

- 5-to-3.3 V level shifting
- 3.3-to-1.8 V level shifting
- Low propagation delay
- TTL control inputs

Applications

- Telecommunications infrastructure
- Memory interleaving
- Industrial control
- Unidirectional level shifting
- Cell phones

CBT(D) selection table

			TSSOP	SSOP	SO	DQFN	MicroPak
Type number	Function	Description	Suffix DGG, PW	Suffix DS, DK	Suffix D	Suffix BQ	Suffix GF, GM, GN, GS
CBT16210	Bus switch	20-bit bus switch	•	•			
CBT16211	Bus switch	24-bit bus switch	•	•			
CBT16212	Bus switch	24-bit bus exchange switch	•	•			
CBT16292	Bus switch	12-bit 2:1 mux/demux	•				
CBT3125	Bus switch	Quad bus switch	•	•	•		
CBT3126	Bus switch	Quad bus switch	•	•	•		
CBT3244A	Bus switch	Octal bus switch	•	•	•	•	
CBT3245A	Bus switch	Octal bus switch	•	•	•	•	
CBT3251	Bus switch	8:1 mux/demux	•	•	•		
CBT3253A	Bus switch	Dual 4:1 mux/demux	•	•	•		
CBT3257A	Bus switch	Quad 2:1 mux/demux	•	•	•	•	
CBT3306	Bus switch	Dual bus switch	•		•		•
CBT3384	Bus switch	10-bit bus switch	•	•	•		
CBT3861	Bus switch	10-bit bus switch	•	•		•	
CBTD16210	Bus switch	20-bit bus switch level translator	•	•			
CBTD3306	Bus switch	Dual bus switch level translator	•		•		•
CBTD3384	Bus switch	10-bit bus switch level translator	•	•	•		
CBTD3861	Bus switch	10-bit bus switch level translator	•	•		•	

Low-voltage families

This section includes the following low-voltage logic families, in ascending order of performance

LV LOGIC

The LV family provides the performance of 5 V HCMOS within the supply range of 3.0 to 3.6 V. The typical operating range is from 1.0 to 3.6 V, but many functions are specified from 1.0 to 5.5 V, with low ground bounce and high reliability. Offering fully compatible TTL input levels and balanced propagation delays for high speed, LV devices deliver higher output drive and higher speed than 5 V HCMOS devices. The family is pin-compatible with HC(T) devices and is fully specified from -40 to +125 °C.

Features and benefits

- Wide operating voltage (1.0 to 5.5 V)
- Optimized for low-voltage applications (1.0 to 3.6 V)
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical high-level output voltage
- (V_{OH}) undershoot: > 2 V at V_{CC}= 3.3 V and T_{amb} = 25 °C

Applications

- Industrial control (linear amplifiers, crystal oscillators, etc.)
- Battery back-up systems (chargers, UPS systems, etc.)
- Electronic data-processing peripherals
- Automotive electrical systems

LV selection table

Type number	Function	Description	TSSOP	SSOP	SO	DQFN
			Suffix PW	Suffix DB	Suffix D	Suffix BQ
74LV00	NAND gate	Quad 2-input NAND gate	•	•	•	•
74LV02	NOR gate	Quad 2-input NOR gate		•	•	•
74LV03	NAND gate	Quad 2-input NAND gate; open drain			•	
74LV04	Buffer/inverter/driver	Hex inverter				•
74LV08	AND gate	Quad 2-input AND gate	•	•	•	
74LV123	Multivibrator	Dual retriggerable monostable multivibrator with reset	•	•	•	•
74LV125	Buffer/inverter/driver	Quad buffer/line driver (3-state)	•	•	•	
74LV132	Schmitt trigger	Quad 2-input NAND gate Schmitt trigger	•	•	•	•
74LV138	Decoder/demultiplexer	3-to-8 line decoder/demultiplexer; inverting	•	•	•	•
74LV139	Decoder/demultiplexer	Dual 2-to-4 line decoder/demultiplexer	•	•	•	•
74LV14	Schmitt trigger	Hex inverter Schmitt trigger	•	•	•	•
74LV153	Digital multiplexer	Dual 4-input multiplexer	•	•	•	
74LV164	Shift register	8-bit serial-in/parallel-out shift register	•	•	•	•
74LV165	Shift register	8-bit parallel or serial-in/serial-out shift register	•	•	•	
74LV165A	Shift register	8-bit parallel or serial-in/serial-out shift register	•		•	
74LV174	D-type flip-flop	Hex D-type flip-flop with reset; positive-edge trigger	•	•	•	
74LV241	Buffer/inverter/driver	Octal buffer/line driver (3-state)	•	•	•	
74LV244	Buffer/inverter/driver	Octal buffer/line driver (3-state)	•	•	•	
74LV245	Transceiver	Octal transceiver (3-state)	•	•	•	
74LV251	Digital multiplexer	8-input multiplexer (3-state)	•	•	•	
74LV259	Latch/registered driver	8 bit addressable latch	•	•	•	•
74LV27	NOR gate	Triple 3-input NOR gate			•	
74LV273	D-type flip-flop	Octal D-type flip-flop with reset; positive-edge trigger	•	•	•	
74LV32	OR gate	Quad 2-input OR gate	•	•	•	•
74LV365	Buffer/inverter/driver	Hex buffer/line driver (3-state)	•	•	•	
74LV367	Buffer/inverter/driver	Hex buffer/line driver (3-state)	•	•	•	
74LV373	Latch/registered driver	Octal D-type transparent latch (3-state)	•	•	•	
74LV374	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•	•	•	
74LV377	D-type flip-flop	Octal D-type flip-flop with data enable; positive-edge trigger	•	•	•	
74LV393	Binary counter/timer	Dual 4-bit binary ripple counter	•	•	•	
74LV4020	Binary counter/timer	14-stage binary ripple counter	•	•	•	
74LV4051	Analog switch	Single-pole, octal-throw analog switch	•	•	•	•
74LV4052	Analog switch	Dual single-pole, quad-throw analog switch	•	•	•	
74LV4053	Analog switch	Triple single-pole, double-throw analog switch	•	•	•	•
74LV4060	Binary counter/timer	14-stage binary ripple counter with oscillator	•	•	•	
74LV4066	Analog switch	Quad single-pole, single-throw analog switch	•	•	•	
74LV4094	Shift register	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	•	•	•	
74LV541	Buffer/inverter/driver	Octal buffer/line driver (3-state)	•	•	•	
74LV573	Latch/registered driver	Octal D-type transparent latch (3-state)	•	•	•	
74LV574	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•	•	•	
74LV595	Shift register	8-bit serial-in/parallel-out shift register with output storage register (3-state)	•	•	•	
74LV74	D-type flip-flop	Dual D-type flip-flop with set and reset; positive-edge trigger	•	•	•	
74LV86	EXCLUSIVE-OR gate	Quad 2-input EXCLUSIVE-OR gate	•	•	•	•
74LVU04	Buffer/inverter/driver	Hex inverter; unbuffered	•	•	•	•

LVC LOGIC

LVC logic is specified over 1.65 to 3.6 V in standard formats, and from 1.65 to 5.5 V in PicoGate packages. With a balanced output drive of 24 mA and a typical propagation delay of 2 ns, and an extensive set of special features, the LVC family is well suited for parallel-interface applications. All LVC devices are fully specified from -40 to 125 °C.

Features and benefits

- Typical propagation delay of 2 ns
- Output drive capability I_{OH} / I_{OL} = ±24 mA
- Low power
- 5 V-tolerant I/O
- Live insertion/extraction permitted
- Buffers and drivers with 30 Ω integrated series termination (optional)
- Bus hold on data inputs (optional)
- Bus-interface functions in 16- and 32-bit versions

Applications

- STBs, DVD players, HDTVs
- Workstations
- Telecom and networking equipment
- Advanced bus interfaces
- Computer peripherals

LVC selection table

			TSSOP	VSSOP	SSOP	SO	DQFN	BGA	MicroPak	PicoGate
Type number	Function	Description	Suffix DGG, PW	Suffix DC	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74LVC162244A	Buffer/inverter/ driver	16-bit buffer/line driver with 30 Ω termination resistors (3-state)	•		•					
74LVCH162244A	Buffer/inverter/ driver	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•		•					
74LVC162245A	Transceiver	16-bit transceiver with 30 Ω termination resistors (3-state)	•		•					
74LVCH162245A	Transceiver	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	•		•					
74LVC162373A	Latch/registered driver	16-bit D-type transparent latch with 30 Ω termination resistors (3-state)	•		•					
74LVCH162373A	Latch/registered driver	16-bit D-type transparent latch with bus hold and 30 Ω termination resistors (3-state)	•		•					
74LVC16244A	Buffer/inverter/ driver	16-bit buffer/line driver (3-state)	•		•		•	•		
74LVCH16244A	Buffer/inverter/ driver	16-bit buffer/line driver with bus hold (3-state)	•							
74LVC16245A	Transceiver	16-bit transceiver (3-state)	•		•			•		
74LVCH16245A	Transceiver	16-bit transceiver with bus hold (3-state)	•		•			•		
74LVC16373A	Latch/registered driver	16-bit D-type transparent latch (3-state)	•		•		•			
74LVCH16373A	Latch/registered driver	16-bit D-type transparent latch with bus hold (3-state)	•		•					
74LVC16374A	D-type flip-flop	16-bit D-type flip-flop; positive-edge trigger (3-state)	•		•		•			
74LVCH16374A	D-type flip-flop	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•		•		•			
74LVC1T45	Level shifter/ translator	Single dual-supply voltage-translating transceiver (3-state)							•	•

LVC selection table (cont.)

Type number	Function	Description	TSSOP	VSSOP	SSOP	SO	DQFN	BGA	MicroPak	PicoGate
			Suffix DGG, PW	Suffix DC	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74LVCH1T45	Level shifter/ translator	Single dual-supply voltage-translating transceiver with bus hold (3-state)							•	•
74LVC244A	Buffer/inverter/ driver	Octal buffer/line driver (3-state)	•		•	•	•			
74LVCH244A	Buffer/inverter/ driver	Octal buffer/line driver with bus hold (3-state)	•		•	•	•			
74LVC245A	Transceiver	Octal transceiver (3-state)	•		•	•	•			
74LVCH245A	Transceiver	Octal transceiver with bus hold (3-state)	•		•	•	•			
74LVC2T45	Level shifter/ translator	Dual-bit dual-supply voltage-translating transceiver (3-state)	•						•	
74LVCH2T45	Level shifter/ translator	Dual-bit dual-supply voltage-translating transceiver with bus hold (3-state)	•						•	
74LVC8T245	Level shifter/ translator	8-bit dual-supply voltage-translating transceiver (3-state)	•				•			
74LVC00A	NAND gate	Quad 2-input NAND gate	•		•	•	•			
74LVC02A	NOR gate	Quad 2-input NOR gate	•		•	•	•			
74LVC04A	Buffer/inverter/ driver	Hex inverter	•		•	•	•			
74LVC06A	Buffer/inverter/ driver	Hex inverter; open drain	•			•	•			
74LVC07A	Buffer/inverter/ driver	Hex buffer; open drain	•			•	•			
74LVC08A	AND gate	Quad 2-input AND gate	•		•	•	•			
74LVC109	JK-type flip-flop	Dual J-/K flip-flop with set and reset; positive-edge trigger	•		•	•				
74LVC10A	NAND gate	Triple 3-input NAND gate	•		•	•	•			
74LVC11	AND gate	Triple 3-input AND gate	•		•	•	•			
74LVC125A	Buffer/inverter/ driver	Quad buffer/line driver (3-state)	•		•	•	•			
74LVC126A	Buffer/inverter/ driver	Quad buffer/line driver (3-state)	•		•	•	•			
74LVC132A	Schmitt trigger	Quad 2-input NAND gate Schmitt trigger	•			•	•			
74LVC138A	Decoder/ demultiplexer	3-to-8 line decoder/ demultiplexer; inverting	•		•	•	•			
74LVC139	Decoder/ demultiplexer	Dual 2-to-4 line decoder/ demultiplexer	•		•	•	•			
74LVC14A	Schmitt trigger	Hex inverter Schmitt trigger	•		•	•	•			
74LVC157A	Digital multiplexer	Quad 2-input multiplexer	•		•	•	•			
74LVC161	Binary counter/ timer	Presettable synchronous 4-bit binary counter; asynchronous reset	•		•	•	•			
74LVC16240A	Buffer/inverter/ driver	16-bit inverter/line driver (3-state)	•		•					
74LVC16241A	Buffer/inverter/ driver	16-bit buffer/line driver (3-state)	•		•					
74LVC163	Binary counter/ timer	Presettable synchronous 4-bit binary counter; synchronous reset	•		•	•	•			

LVC selection table (cont.)

			TSSOP	VSSOP	SSOP	SO	DQFN	BGA	MicroPak	PicoGate
Type number	Function	Description	Suffix DGG, PW	Suffix DC	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74LVC169	Binary counter/ timer	Presettable synchronous 4-bit binary up/down counter	•		•	•	•			
74LVC1G00	NAND gate	Single 2-input NAND gate							•	•
74LVC1G02	NOR gate	Single 2-input NOR gate							•	•
74LVC1G04	Buffer/inverter/ driver	Single inverter							•	•
74LVC1G06	Buffer/inverter/ driver	Single inverter; open drain							•	•
74LVC1G07	Buffer/inverter/ driver	Single buffer; open drain							•	•
74LVC1G08	AND gate	Single 2-input AND gate							•	•
74LVC1G10	NAND gate	Single 3-input NAND gate							•	•
74LVC1G11	AND gate	Single 3-input AND gate							•	•
74LVC1G123	Multivibrator	Single retriggerable monostable multivibrator		•					•	•
74LVC1G126	Buffer/inverter/ driver	Single buffer/line driver (3-state)							•	•
74LVC1G14	Schmitt trigger	Single inverter Schmitt trigger							•	•
74LVC1G157	Digital multiplexer	Single 2-input multiplexer							•	•
74LVC1G17	Schmitt trigger	Single buffer Schmitt trigger							•	•
74LVC1G18	Decoder/ demultiplexer	1-to-2 demultiplexer (3-state)							•	•
74LVC1G19	Decoder/ demultiplexer	1-to-2 decoder/demultiplexer							•	•
74LVC1G27	NOR gate	Single 3-input NOR gate							•	•
74LVC1G3157	Analog switch	Single-pole, double-throw analog switch							•	•
74LVC1G32	OR gate	Single 2-input OR gate							•	•
74LVC1G332	OR gate	Single 3-input OR gate							•	•
74LVC1G34	Buffer/inverter/ driver	Single buffer							•	•
74LVC1G38	NAND gate	Single 2-input NAND gate; open drain							•	•
74LVC1G384	Analog switch	Single-pole, Single-throw analog switch							•	•
74LVC1G386	EXCLUSIVE-OR gate	Single 3-Input EXCLUSIVE-OR gate							•	•
74LVC1G53	Analog switch	Single-pole, double-throw analog switch	•	•					•	
74LVC1G57	Configurable multi-function gate	Configurable gate; Schmitt trigger							•	•
74LVC1G58	Configurable multi-function gate	Configurable gate; Schmitt trigger							•	•
74LVC1G66	Analog switch	Single-pole, Single-throw analog switch	•						•	•
74LVC1G74	D-type flip-flop	Single D-type flip-flop with set and reset; positive-edge trigger	•						•	•
74LVC1G79	D-type flip-flop	Single D-type flip-flop; positive-edge trigger	•						•	•

LVC selection table (cont.)

Type number	Function	Description	TSSOP	VSSOP	SSOP	SO	DQFN	BGA	MicroPak	PicoGate
			Suffix DGG, PW	Suffix DC	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74LVC1G80	D-type flip-flop	Single D-type flip-flop; positive-edge trigger	•						•	•
74LVC1G86	EXCLUSIVE-OR gate	Single 2-input EXCLUSIVE-OR gate	•						•	•
74LVC1G97	Configurable multi-function gate	Configurable gate; Schmitt trigger	•						•	•
74LVC1G98	Configurable multi-function gate	Configurable gate; Schmitt trigger	•						•	•
74LVC1G99	Configurable multi-function gate	Configurable gate; Schmitt trigger	•						•	•
74LVC1GU04	Buffer/inverter/ driver	Single inverter; unbuffered	•						•	•
74LVC2244A	Buffer/inverter/ driver	Octal buffer/line driver with 30 Ω termination resistors (3-state)	•		•	•	•			
74LVC2245A	Transceiver	Octal transceiver with 30 Ω termination resistors (3-state)	•		•	•	•			
74LVC240A	Buffer/inverter/ driver	Octal inverter/line driver (3-state)	•		•	•	•			
74LVC241A	Buffer/inverter/ driver	Octal buffer/line driver (3-state)	•		•	•	•			
74LVC257A	Digital multiplexer	Quad 2-input multiplexer (3-state)	•		•	•	•			
74LVC27	NOR gate	Triple 3-input NOR gate	•		•	•	•			
74LVC273	D-type flip-flop	Octal D-type flip-flop with reset; positive-edge trigger	•		•	•	•			
74LVC2952A	Transceiver	Octal registered transceiver with 30 Ω termination resistors (3-state)	•		•	•	•			
74LVC2G00	NAND gate	Dual 2-input NAND gate	•	•					•	•
74LVC2G02	NOR gate	Dual 2-input NOR gate	•	•					•	•
74LVC2G04	Buffer/inverter/ driver	Dual inverter	•	•					•	•
74LVC2G06	Buffer/inverter/ driver	Dual inverter; open drain	•	•					•	•
74LVC2G07	Buffer/inverter/ driver	Dual buffer; open drain	•	•					•	•
74LVC2G08	AND gate	Dual 2-input AND gate	•	•					•	•
74LVC2G125	Buffer/inverter/ driver	Dual buffer/line driver; TTL-enabled (3-state)	•	•					•	•
74LVC2G126	Buffer/inverter/ driver	Dual buffer/line driver; TTL-enabled (3-state)	•	•					•	•
74LVC2G14	Schmitt trigger	Dual inverter Schmitt trigger	•						•	•
74LVC2G17	Schmitt trigger	Dual buffer Schmitt trigger	•						•	•
74LVC2G240	Buffer/inverter/ driver	Dual inverter/line driver (3-state)	•	•					•	•
74LVC2G241	Buffer/inverter/ driver	Dual buffer/line driver (3-state)	•	•					•	•
74LVC2G32	OR gate	Dual 2-input OR gate	•	•					•	•
74LVC2G34	Buffer/inverter/ driver	Dual buffer	•	•					•	•

LVC selection table (cont.)

Type number	Function	Description	TSSOP Suffix DGG, PW	VSSOP Suffix DC	SSOP Suffix DB, DL	SO Suffix D	DQFN Suffix BQ, BX	BGA Suffix EC, EV	MicroPak Suffix GD, GF, GM, GN, GS, GT, GX	PicoGate Suffix DP, GW, GV
74LVC2G38	NAND gate	Dual 2-input NAND gate; open drain	•	•					•	•
74LVC2G53	Analog switch	Single-pole, double-throw analog switch	•	•					•	•
74LVC2G66	Analog switch	Dual single-pole, single-throw analog switch	•	•					•	•
74LVC2G74	D-type flip-flop	Single D-type flip-flop with set and reset; positive-edge trigger	•	•					•	•
74LVC2G86	EXCLUSIVE-OR gate	Dual 2-input EXCLUSIVE-OR gate	•	•					•	•
74LVC2GU04	Buffer/inverter/ driver	Dual inverter; unbuffered	•	•					•	•
74LVC32245A	Transceiver	32-bit transceiver (3-state)						•		
74LVC32A	OR gate	Quad 2-input OR gate	•		•	•	•			
74LVC373A	Latch/registered driver	Octal D-type transparent latch (3-state)	•		•	•	•			
74LVC374A	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•		•	•	•			
74LVC377	D-type flip-flop	Octal D-type flip-flop with data enable; positive-edge trigger	•		•	•				
74LVC38A	NAND gate	Quad 2-input NAND gate; open drain	•		•	•	•			
74LVC3G04	Buffer/inverter/ driver	Triple inverter	•	•					•	
74LVC3G06	Buffer/inverter/ driver	Triple inverter; open drain	•	•					•	
74LVC3G07	Buffer/inverter/ driver	Triple buffer; open drain	•	•					•	
74LVC3G14	Schmitt trigger	Triple inverter Schmitt trigger	•	•					•	
74LVC3G17	Schmitt trigger	Triple buffer Schmitt trigger	•	•					•	
74LVC3G34	Buffer/inverter/ driver	Triple buffer	•	•					•	
74LVC3GU04	Buffer/inverter/ driver	Triple inverter; unbuffered	•	•					•	
74LVC4066	Analog switch	Quad single-pole, single-throw analog switch	•			•	•			
74LVC4245A	Level shifter/ translator	8-bit dual-supply voltage-translating transceiver (3-state)	•			•	•			
74LVC541A	Buffer/inverter/ driver	Octal buffer/line driver (3-state)	•		•	•	•			
74LVC543A	Transceiver	Octal registered transceiver (3-state)	•		•	•	•			
74LVC544A	Transceiver	Octal registered transceiver; inverting (3-state)	•			•	•			
74LVC573A	Latch/registered driver	Octal D-type transparent latch (3-state)	•			•	•			
74LVC574A	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•		•	•	•			
74LVC594A	Shift register	8-bit serial-in/parallel-out shift register with output storage register	•			•	•			

LVC selection table (cont.)

Type number	Function	Description	TSSOP	VSSOP	SSOP	SO	DQFN	BGA	MicroPak	PicoGate
			Suffix DGG, PW	Suffix DC	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74LVC595A	Shift register	8-bit serial-in/parallel-out shift register with output storage register (3-state)	•			•	•			
74LVC623A	Transceiver	Octal transceiver with dual enable (3-state)	•			•	•			
74LVC646A	Transceiver	Octal registered transceiver (3-state)	•			•				
74LVC74A	D-type flip-flop	Dual D-type flip-flop with set and reset; positive-edge trigger	•		•	•	•			
74LVC821A	D-type flip-flop	10-bit D-type flip-flop; positive-edge trigger (3-state)	•		•	•	•			
74LVC827A	Buffer/inverter/ driver	10-bit buffer/line driver (3-state)	•		•	•	•			
74LVC841A	Latch/registered driver	10-bit D-type transparent latch (3-state)	•		•	•	•			
74LVC86A	EXCLUSIVE-OR gate	Quad 2-input EXCLUSIVE-OR gate	•		•	•	•			
74LVCH162374A	D-type flip-flop	16-bit D-type flip-flop with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	•		•					
74LVCH16541A	Buffer/inverter/ driver	16-bit buffer/line driver with bus hold (3-state)	•		•					
74LVCH322244A	Buffer/inverter/ driver	32-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)						•		
74LVCH322245A	Transceiver	32-bit transceiver with bus hold and 30 Ω termination resistors (3-state)						•		
74LVCH32244A	Buffer/inverter/ driver	32-bit buffer/line driver with bus hold (3-state)						•		
74LVCH32245A	Transceiver	32-bit transceiver with bus hold (3-state)						•		
74LVCH32373A	Latch/registered driver	32-bit D-type transparent latch (3-state)						•		
74LVCH32374A	D-type flip-flop	32-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)						•		
74LVCU04A	Buffer/inverter/ driver	Hex inverter; unbuffered	•				•			
74LVCV2G66	Analog switch	Dual single-pole, single-throw analog switch; overvoltage tolerant		•						•

ALVC LOGIC

ALVC logic devices are specified over a voltage range of 1.65 to 3.6 V. They have a balanced output drive of 24 mA and a typical propagation delay of 2 ns, and are well suited for parallel-interface applications. ALVC products are fully specified from -40 to 85 °C.

Features and benefits

Typical propagation delay of 2 ns
Output drive capability I_{OH} / I_{OL} = ±24 mA
Low power
3.6 V-tolerant I/O
Live insertion/extraction permitted
Buffers and drivers with 30 Ω integrated series termination (optional)
Bus hold on data inputs (optional)
Bus-interface functions in 16- and 32-bit versions

Applications

STBs, DVD players, HDTVs
Workstations
Telecom and networking equipment
Advanced bus interfaces
Computer peripherals

ALVC selection table

			TSSOP	SSOP	QFN	BGA
Type number	Function	Description	Suffix DGG, PW	Suffix D, DL	Suffix BQ, BX	Suffix EC
74ALVC16244	Buffer/inverter/driver	16-bit buffer/line driver (3-state)	•	•		
74ALVCH16244	Buffer/inverter/driver	16-bit buffer/line driver with bus hold (3-state)	•	•		
74ALVC16245	Transceiver	16-bit transceiver (3-state)	•	•		
74ALVCH16245	Transceiver	16-bit transceiver with bus hold (3-state)	•	•		
74ALVC00	NAND gate	Quad 2-input NAND gate	•	•	•	
74ALVC02	NOR gate	Quad 2-input NOR gate	•	•	•	
74ALVC04	Buffer/inverter/driver	Hex inverter	•	•	•	
74ALVC08	AND gate	Quad 2-input AND gate	•	•	•	
74ALVC125	Buffer/inverter/driver	Quad buffer/line driver (3-state)	•	•	•	
74ALVC14	Schmitt trigger	Hex inverter Schmitt trigger	•	•	•	
74ALVC162334A	Latch/registered driver	16-bit registered driver with 30 Ω termination resistors (3-state)	•	•	•	
74ALVC162834A	Latch/registered driver	18-bit registered driver with 30 Ω termination resistors (3-state)	•	•	•	
74ALVC164245	Level shifter/translator	16-bit dual-supply voltage-translating transceiver (3-state)	•	•	•	
74ALVC16834A	Latch/registered driver	18-bit registered driver (3-state)	•	•	•	
74ALVC16835A	Latch/registered driver	18-bit registered driver (3-state)	•	•	•	
74ALVC16836A	Latch/registered driver	20-bit registered driver (3-state)	•	•	•	
74ALVC244	Buffer/inverter/driver	Octal buffer/line driver (3-state)	•	•	•	
74ALVC245	Transceiver	Octal transceiver (3-state)	•	•	•	
74ALVC32	OR gate	Quad 2-input OR gate	•	•	•	

ALVC selection table (cont.)

Type number	Function	Description	TSSOP	SSOP	QFN	BGA
			Suffix DGG, PW	Suffix D, DL	Suffix BQ, BX	Suffix EC
74ALVC373	Latch/registered driver	Octal D-type transparent latch (3-state)	•	•	•	
74ALVC541	Buffer/inverter/driver	Octal buffer/line driver (3-state)	•	•	•	
74ALVC573	Latch/registered driver	Octal D-type transparent latch (3-state)	•	•	•	
74ALVC574	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•	•	•	
74ALVC74	D-type flip-flop	Dual D-type flip-flop with set and reset; positive-edge trigger	•	•	•	
74ALVCH162245	Transceiver	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	•	•		
74ALVCH162601	Transceiver	18-bit universal bus transceiver with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	•			
74ALVCH162827	Buffer/inverter/driver	20-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•			
74ALVCH16373	Latch/registered driver	16-bit D-type transparent latch with bus hold (3-state)	•	•		
74ALVCH16374	D-type flip-flop	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•	•		
74ALVCH16500	Transceiver	18-bit universal bus transceiver with bus hold; negative edge trigger (3-state)	•			
74ALVCH16501	Transceiver	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	•	•		
74ALVCH16543	Transceiver	16-bit registered transceiver with bus hold (3-state)	•			
74ALVCH16600	Transceiver	18-bit universal bus transceiver with bus hold; negative edge trigger (3-state)	•			
74ALVCH16601	Transceiver	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	•			
74ALVCH16646	Transceiver	16-bit registered transceiver with bus hold (3-state)	•			
74ALVCH16652	Transceiver	16-bit registered transceiver with bus hold (3-state)	•			
74ALVCH16821	D-type flip-flop	20-bit D-type flip-flop; positive-edge trigger (3-state)	•	•		
74ALVCH16823	D-type flip-flop	18-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•	•		
74ALVCH16825	Buffer/inverter/driver	18-bit buffer/line driver with bus hold (3-state)	•			
74ALVCH16827	Buffer/inverter/driver	20-bit buffer/line driver with bus hold (3-state)	•			
74ALVCH16832	Latch/registered driver	7-bit to 28-bit address register/driver (3-state)	•			
74ALVCH16841	Latch/registered driver	20-bit D-type transparent latch with bus hold (3-state)	•			
74ALVCH16843	Latch/registered driver	18-bit D-type transparent latch with bus hold (3-state)	•			
74ALVCH16952	Transceiver	16-bit registered transceiver with bus hold (3-state)	•			
74ALVCH32973	Latch/registered driver	16-bit transceiver and transparent D-type latch with 8 independent buffers	•			•

LVT LOGIC

The LVT family combines the low power dissipation and low noise of CMOS with the high speed and high output drive of bipolar products. LVT devices exhibit highly stable static and dynamic characteristics over a wide temperature range, are specified over 2.7 to 3.6 V, and support live insertion. With output drive as high as 64 mA and typical propagation delay of 2 ns, these devices are well suited for parallel-backplane applications. They are fully specified from -40 °C to 85 °C.

Features and benefits

- Typical propagation delay of 2 ns
- Output drive capability I_{OH} / I_{OL} = -32/+64 mA
- Supply voltage range V_{CC} = 2.7 to 3.6 V
- 5 V-tolerant I/O
- Bus hold on data inputs
- Power-up/power-down 3-state
- Live insertion
- Buffers and drivers with 30 Ω integrated series termination (optional)

Applications

- Backplane drivers
- Workstations
- Telecom and networking equipment
- Advanced bus interfaces
- Computer peripherals

LVT selection table

			TSSOP	SSOP	SO	QFN	BGA
Type number	Function	Description	Suffix DGG, PW	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV
74LVT125	Buffer/inverter/driver	Quad buffer/line driver with bus hold (3-state)	•	•	•	•	
74LVTH125	Buffer/inverter/driver	Quad buffer/line driver with bus hold (3-state)	•	•	•	•	
74LVT16244B	Buffer/inverter/driver	16-bit buffer/line driver with bus hold (3-state)	•	•		•	•
74LVTH16244B	Buffer/inverter/driver	16-bit buffer/line driver with bus hold (3-state)	•	•		•	
74LVT16245B	Transceiver	16-bit transceiver with bus hold (3-state)	•	•		•	•
74LVTH16245B	Transceiver	16-bit transceiver with bus hold (3-state)	•	•		•	
74LVT16374A	D-type flip-flop	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•	•		•	•
74LVTH16374A	D-type flip-flop	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)					•
74LVT2245	Transceiver	Octal transceiver with bus hold and 30 Ω termination resistors (3-state)	•	•		•	
74LVTH2245	Transceiver	Octal transceiver with bus hold and 30 Ω termination resistors (3-state)	•	•		•	
74LVT244A	Buffer/inverter/driver	Octal buffer/line driver with bus hold (3-state)	•	•		•	
74LVTH244A	Buffer/inverter/driver	Octal buffer/line driver with bus hold (3-state)	•	•		•	
74LVT244B	Buffer/inverter/driver	Octal buffer/line driver with bus hold (3-state)	•	•	•		
74LVTH244B	Buffer/inverter/driver	Octal buffer/line driver with bus hold (3-state)	•	•	•		
74LVT574	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•	•	•		
74LVTH574	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•	•	•		
74LVT00	NAND gate	Quad 2-input NAND gate	•	•	•		
74LVT02	NOR gate	Quad 2-input NOR gate	•	•	•		
74LVT04	Buffer/inverter/driver	Hex inverter	•	•	•		
74LVT08	AND gate	Quad 2-input AND gate	•	•	•		
74LVT10	NAND gate	Triple 3-input NAND gate	•	•	•		
74LVT126	Buffer/inverter/driver	Quad buffer/line driver with bus hold (3-state)	•	•	•	•	
74LVT14	Schmitt trigger	Hex inverter Schmitt trigger	•	•	•	•	
74LVT162240A	Buffer/inverter/driver	16-bit inverter/line driver with bus hold and 30 Ω termination (3-state)	•	•			

LVT selection table (cont.)

Type number	Function	Description	TSSOP	SSOP	SO	QFN	BGA
			Suffix DGG, PW	Suffix DB, DL	Suffix D	Suffix BQ, BX	Suffix EC, EV
74LVT162244B	Buffer/inverter/driver	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•			
74LVT162245B	Transceiver	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	•	•			
74LVT162373	Latch/registered driver	16-bit D-type transparent latch with bus hold and 30 Ω termination resistors (3-state)	•	•			
74LVT162374	D-type flip-flop	16-bit D-type flip-flop with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	•	•			
74LVT16240A	Buffer/inverter/driver	16-bit inverter/line driver with bus hold (3-state)	•	•			
74LVT16373A	Latch/registered driver	16-bit D-type transparent latch with bus hold (3-state)	•	•			
74LVT16500A	Transceiver	18-bit universal bus transceiver with bus hold; negative-edge trigger (3-state)	•	•			
74LVT16501A	Transceiver	18-bit universal bus transceiver with bus hold; positive-edge trigger (3-state)	•	•			
74LVT16543A	Transceiver	16-bit registered transceiver with bus hold (3-state)	•	•			
74LVT16646A	Transceiver	16-bit registered transceiver with bus hold (3-state)	•	•			
74LVT16652A	Transceiver	16-bit registered transceiver with bus hold (3-state)	•	•	•		
74LVT2241	Buffer/inverter/driver	Octal buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•	•		
74LVT2244	Buffer/inverter/driver	Octal buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•	•		
74LVT240	Buffer/inverter/driver	Octal inverter/line driver with bus hold (3-state)	•	•	•		
74LVT241	Buffer/inverter/driver	Octal buffer/line driver with bus hold (3-state)	•	•	•	•	
74LVT245B	Transceiver	Octal transceiver (3-state)	•	•	•	•	
74LVT245	Transceiver	Octal transceiver (3-state)	•	•	•	•	
74LVT273	D-type flip-flop	Octal D-type flip-flop with reset; positive-edge trigger	•	•	•	•	
74LVT2952	Transceiver	Octal registered transceiver with 30 Ω termination resistors (3-state)	•	•	•		
74LVT32	OR gate	Quad 2-input OR gate	•	•	•		
74LVT32374	D-type flip-flop	32-bit D-type flip-flop with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)					•
74LVT373	D-type flip-flop	Octal D-type transparent latch (3-state)	•		•		
74LVT374	D-type flip-flop	Octal D-type flip-flop; positive-edge trigger (3-state)	•	•	•		
74LVT534	D-type flip-flop	Octal D-type flip-flop; inverting; positive-edge trigger (3-state)	•	•	•		
74LVT543	Transceiver	Octal registered transceiver (3-state)	•	•	•		
74LVT573	Latch/registered driver	Octal D-type transparent latch (3-state)	•	•	•	•	
74LVT640	Transceiver	Octal transceiver with bus hold; inverting (3-state)	•	•	•		
74LVT646	Transceiver	Octal registered transceiver with bus hold (3-state)	•	•	•		
74LVT652	Transceiver	Octal registered transceiver with bus hold (3-state)	•	•	•		
74LVT74	D-type flip-flop	Dual D-type flip-flop with set and reset; positive-edge trigger	•	•	•		
74LVTH322245	Transceiver	32-bit transceiver with bus hold and 30 Ω termination resistors (3-state)					•
74LVTH32245	Transceiver	32-bit transceiver with bus hold (3-state)					•
74LVTN16244B	Buffer/inverter/driver	16-bit buffer/line driver (3-state)	•			•	
74LVTN16245B	Transceiver	16-bit transceiver (3-state)	•			•	

ALVT LOGIC

The ALVT family is a speed upgrade for the LVT family. It combines the low power dissipation and low noise of CMOS with the high speed and high output drive of bipolar products. ALVT devices exhibit highly stable static and dynamic characteristics over a wide temperature range, are specified over 2.7 to 3.6 V, and support live insertion. With output drive as high as 64 mA and typical propagation delay of 2 ns, these devices are well suited for parallel-backplane applications. They are fully specified from -40 °C to 85 °C.

Features and benefits

- Typical propagation delay of 1.5 ns
- Output drive capability I_{OH} / I_{OL} = -32/+64 mA
- Supply voltage range V_{CC} = 2.7 to 3.6 V
- 5 V-tolerant I/O
- Bus hold on data inputs
- Power-up/power-down 3-state
- Live insertion
- Buffers and drivers with 30 Ω integrated series termination (optional)

Applications

- Backplane drivers
- Workstations
- Telecom and networking equipment
- Advanced bus interfaces
- Computer peripherals

ALVT selection table

			TSSOP	SSOP
Type number	Function	Description	Suffix DGG	Suffix DL
74ALVT162240	Buffer/inverter/driver	16-bit inverter/line driver with bus hold and 30 Ω termination (3-state)	•	•
74ALVT162241	Buffer/inverter/driver	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•
74ALVT162244	Buffer/inverter/driver	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•
74ALVT162245	Transceiver	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	•	•
74ALVT16240	Buffer/inverter/driver	16-bit inverter/line driver with bus hold (3-state)	•	•
74ALVT16241	Buffer/inverter/driver	16-bit buffer/line driver with bus hold (3-state)	•	•
74ALVT16244	Buffer/inverter/driver	16-bit buffer/line driver with bus hold (3-state)	•	•
74ALVT16245	Transceiver	16-bit transceiver with bus hold (3-state)	•	•
74ALVT16260	Latch/registered driver	12-bit to 24-bit multiplexed D-type latch with bus hold (3-state)	•	•
74ALVT162821	D-type flip-flop	20-bit D-type flip-flop; positive-edge trigger (3-state)	•	•
74ALVT162823	D-type flip-flop	18-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•
74ALVT162827	Buffer/inverter/driver	20-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	•	•
74ALVT16373	Latch/registered driver	16-bit D-type transparent latch with bus hold (3-state)	•	•
74ALVT16374	D-type flip-flop	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•	•
74ALVT16501	Transceiver	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	•	•
74ALVT16543	Transceiver	16-bit registered transceiver with bus hold (3-state)	•	•
74ALVT16601	Transceiver	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	•	•
74ALVT16652	Transceiver	16-bit registered transceiver with bus hold (3-state)	•	•
74ALVT16821	D-type flip-flop	20-bit D-type flip-flop; positive-edge trigger (3-state)	•	•
74ALVT16823	D-type flip-flop	18-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	•	•
74ALVT16827	Buffer/inverter/driver	20-bit buffer/line driver with bus hold (3-state)	•	•

AVC(M) LOGIC

AVC and AVCM devices are advanced, very low-voltage CMOS logic. With a typical propagation delay of 1.5 ns, AVC and AVCM devices are some of the fastest logic devices in the industry. To reduce under- and overshoots at outputs, the AVCM has a source-terminated, balanced drive of 12 mA drive. AVCM devices also use dynamically controlled outputs (DCO) to increase output impedance after the output transition is completed. The result is termination with a high signal rate. The parallel-interface products are fully specified from -40 to +85 °C. The dual-supply transceivers for level translation are fully specified from -40 to +125 °C.

Features and benefits

- Typical propagation delay of 1.5 ns
- Dynamically controlled outputs
- Wide supply range (1.2 to 3.6 V)
- 3.6 V-tolerant I/O
- I_{OFF} supports partial power-down mode
- Buffers and drivers with 15 Ω integrated series termination (optional)
- Bus hold on data inputs (optional)
- Dual-supply level translation
- Bus-interface functions in 16-bit versions

Applications

- High-end workstations, servers, and desktop PCs
- High-end telecommunications switching equipment
- Telecommunication basestations
- Memory modules
- Voltage-level translation

AVC(M) selection table

			TSSOP	VSSOP	SO	QFN	BGA	MicroPak	PicoGate
Type number	Function	Description	Suffix DGG, PW	Suffix DC	Suffix D	Suffix BQ, BX, GU	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74AVC16244	Buffer/inverter/driver	16-bit buffer/line driver (3-state)	•						
74AVC16334A	Latch/registered driver	16-bit registered driver (3-state)	•						
74AVC16373	Latch/registered driver	16-bit D-type transparent latch (3-state)	•						
74AVC16374	D-type flip-flop	16-bit D-type flip-flop; positive-edge trigger (3-state)	•						
74AVC16834A	Latch/registered driver	18-bit registered driver (3-state)	•						
74AVC16835A	Latch/registered driver	18-bit registered driver (3-state)	•						
74AVC16836A	Latch/registered driver	20-bit registered driver (3-state)	•						
74AVC16T245	Level shifter/translator	16-bit dual-supply voltage-translating transceiver (3-state)	•			•	•		
74AVC1T45	Level shifter/translator	Single dual-supply voltage-translating transceiver (3-state)						•	•
74AVC20T245	Level shifter/translator	20-bit dual-supply voltage-translating transceiver (3-state)	•			•			
74AVC2T45	Level shifter/translator	Dual-bit dual-supply voltage-translating transceiver (3-state)		•		•		•	•
74AVC32T245	Level shifter/translator	32-bit dual-supply voltage-translating transceiver (3-state)					•		
74AVC4T245	Level shifter/translator	4-bit dual-supply voltage-translating transceiver (3-state)			•	•			
74AVC4TD245	Level shifter/translator	4-bit dual-supply voltage-translating transceiver (3-state)			•	•			
74AVC8T245	Level shifter/translator	8-bit dual-supply voltage-translating transceiver (3-state)	•			•			
74AVCH16244	Buffer/inverter/driver	16-bit buffer/line driver with bus hold (3-state)	•		•	•			
74AVCH16T245	Level shifter/translator	16-bit dual-supply voltage-translating transceiver with bus hold (3-state)	•				•		
74AVCH1T45	Level shifter/translator	Single dual-supply voltage-translating transceiver with bus hold (3-state)						•	

AVC(M) selection table (cont.)

Type number	Function	Description	TSSOP	VSSOP	SO	QFN	BGA	MicroPak	PicoGate
			Suffix DGG, PW	Suffix DC	Suffix D	Suffix BQ, BX, GU	Suffix EC, EV	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74AVCH20T245	Level shifter/translator	20-bit dual-supply voltage-translating transceiver with bus hold (3-state)	•						
74AVCH2T45	Level shifter/translator	Dual-bit dual-supply voltage-translating transceiver with bus hold (3-state)		•				•	•
74AVCH4T245	Level shifter/translator	4-bit dual-supply voltage-translating transceiver with bus hold (3-state)	•		•	•			
74AVCH8T245	Level shifter/translator	8-bit dual-supply voltage-translating transceiver with bus hold (3-state)	•			•			
74AVCM162834	Latch/registered driver	18-bit registered driver with 30 Ω termination resistors (3-state)	•						
74AVCM162835	Latch/registered driver	18-bit registered driver with 15 Ω termination resistors (3-state)	•						
74AVCM162836	Latch/registered driver	20-bit registered driver with 15 Ω termination resistors (3-state)	•						

AUP LOGIC

The AUP family is the industry standard for portable applications. It is manufactured in a CMOS process that results in lower static and dynamic power dissipation. It's 3.6 V tolerance, low-threshold inputs (option) and I_{OFF} features make it suitable for use in mixed 1.8/3.3 V and partial power-down applications. The family is fully specified from 1.1 to 3.6 V and is guaranteed for industrial and automotive operating temperatures.

Features and benefits

- Very low dynamic power dissipation (C_{PD})
- Wide supply voltage V_{CC} (0.8 to 3.6 V)
- Schmitt-trigger action provides high noise immunity
- Superior ESD protection
- Wide operating temperature of -40 to +125 °C
- t_{PD} of 3.2 ns and I_{OL} of 2.2 mA at 1.8 V V_{CC}

Applications

- Mobile phones
- PDAs
- Digital cameras
- Media players
- Portable medical devices
- Other handheld, power-sensitive applications

AUP selection table

Type number	Function	Description	VSSOP	MicroPak	PicoGate
			Suffix DC	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74AUP1G00	NAND gate	Single 2-input NAND gate		•	•
74AUP1G04	Buffer/inverter/driver	Single inverter		•	•
74AUP1G06	Buffer/inverter/driver	Single inverter; open drain		•	•
74AUP1G07	Buffer/inverter/driver	Single buffer; open drain		•	•
74AUP1G08	AND gate	Single 2-input AND gate		•	•
74AUP1G0832	Combination gate	Single 3-input AND-OR gate		•	•
74AUP1G09	AND gate	Single 2-input AND gate; open drain		•	•

AUP selection table (cont.)

Type number	Function	Description	VSSOP	MicroPak	PicoGate
			Suffix DC	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74AUP1G11	AND gate	Single 3-input AND gate		•	•
74AUP1G125	Buffer/inverter/driver	Single buffer/line driver (3-state)		•	•
74AUP1G126	Buffer/inverter/driver	Single buffer/line driver (3-state)		•	•
74AUP1G132	NAND gate	Single 2-input NAND gate Schmitt trigger		•	•
74AUP1G14	Buffer/inverter/driver	Single inverter; Schmitt trigger		•	•
74AUP1G157	Digital multiplexer	Single 2-input multiplexer		•	•
74AUP1G158	Digital multiplexer	Single 2-input multiplexer; inverting		•	•
74AUP1G17	Schmitt trigger	Single buffer Schmitt trigger		•	•
74AUP1G175	D-type flip-flop	Single D flip-flop with reset; positive-edge trigger		•	•
74AUP1G18	Decoder/demultiplexer	1-to-2 demultiplexer (3-state)		•	•
74AUP1G19	Decoder/demultiplexer	1-to-2 decoder/demultiplexer		•	•
74AUP1G240	Buffer/inverter/driver	Single inverter/line driver (3-state)		•	•
74AUP1G32	OR gate	Single 2-input OR gate		•	•
74AUP1G3208	Combination gate	Single 3-input OR-AND gate		•	•
74AUP1G332	OR gate	Single 3-input OR gate		•	•
74AUP1G34	Buffer/inverter/driver	Single buffer		•	•
74AUP1G373	Latch/registered driver	Single D-type transparent latch (3-state)		•	•
74AUP1G374	D-type flip-flop	Single D-type flip-flop; positive-edge trigger (3-state)		•	•
74AUP1G38	NAND gate	Single 2-input NAND gate; open drain		•	•
74AUP1G386	EXCLUSIVE-OR gate	Single 3-input EXCLUSIVE-OR gate		•	•
74AUP1G57	Configurable multi-function gate	Configurable gate; Schmitt trigger		•	•
74AUP1G58	Configurable multi-function gate	Configurable gate; Schmitt trigger		•	•
74AUP1G74	D-type flip-flop	Single D-type flip-flop with set and reset; positive-edge trigger		•	•
74AUP1G79	D-type flip-flop	Single D-type flip-flop; positive-edge trigger		•	•
74AUP1G80	D-type flip-flop	Single D-type flip-flop; positive-edge trigger		•	•
74AUP1G86	EXCLUSIVE-OR gate	Single 2-input EXCLUSIVE-OR gate		•	•
74AUP1G885	Combination gate	Dual function gate		•	•
74AUP1G97	Configurable multi-function gate	Configurable gate; Schmitt trigger		•	•
74AUP1G98	Configurable multi-function gate	Configurable gate; Schmitt trigger		•	•
74AUP1GU04	Buffer/inverter/driver	Single inverter; unbuffered		•	•
74AUP1T34	Level shifter/translator	Single dual-supply translating buffer		•	•
74AUP1T45	Level shifter/translator	Single dual-supply voltage-translating transceiver (3-state)		•	•
74AUP1T57	Configurable multi-function gate	Configurable gate with voltage level translation		•	•

AUP selection table (cont.)

Type number	Function	Description	VSSOP	MicroPak	PicoGate
			Suffix DC	Suffix GD, GF, GM, GN, GS, GT, GX	Suffix DP, GW, GV
74AUP1T58	Configurable multi-function gate	Configurable gate with voltage level translation		•	•
74AUP1T97	Configurable multi-function gate	Configurable gate with voltage level translation		•	•
74AUP1T98	Configurable multi-function gate	Configurable gate with voltage level translation		•	•
74AUP1Z04	Combination gate	Crystal driver with enable and internal resistor		•	•
74AUP1Z125	Combination gate	Crystal driver with enable and internal resistor (3-state)		•	•
74AUP2G00	NAND gate	Dual 2-input NAND gate	•	•	•
74AUP2G02	NOR gate	Dual 2-input NOR gate	•	•	•
74AUP2G04	Buffer/inverter/driver	Dual inverter		•	•
74AUP2G06	Buffer/inverter/driver	Dual inverter; open drain		•	•
74AUP2G0604	Combination gate	Inverter with open drain and inverter		•	•
74AUP2G07	Buffer/inverter/driver	Dual buffer; open drain		•	•
74AUP2G08	AND gate	Dual 2-input AND gate	•	•	•
74AUP2G125	Buffer/inverter/driver	Dual buffer/line driver (3-state)	•	•	•
74AUP2G126	Buffer/inverter/driver	Dual buffer/line driver (3-state)	•	•	•
74AUP2G132	Schmitt trigger	Dual 2-input NAND gate Schmitt trigger	•	•	•
74AUP2G14	Buffer/inverter/driver	Dual inverter; Schmitt trigger	•	•	•
74AUP2G157	Digital multiplexer	Single 2-input multiplexer	•	•	•
74AUP2G17	Schmitt trigger	Dual buffer Schmitt trigger	•	•	•
74AUP2G240	Buffer/inverter/driver	Dual inverter/line driver (3-state)	•	•	•
74AUP2G241	Buffer/inverter/driver	Dual buffer/line driver (3-state)	•	•	•
74AUP2G32	OR gate	Dual 2-input OR gate	•	•	•
74AUP2G34	Buffer/inverter/driver	Dual buffer	•	•	•
74AUP2G3404	Combination gate	Buffer and inverter	•	•	•
74AUP2G3407	Combination gate	Buffer and buffer with open drain	•	•	•
74AUP2G38	NAND gate	Dual 2-input NAND gate; open drain	•	•	•
74AUP2G79	D-type flip-flop	Dual D-type flip-flop; positive-edge trigger	•	•	•
74AUP2G80	D-type flip-flop	Dual D-type flip-flop; positive-edge trigger	•	•	•
74AUP2G86	EXCLUSIVE-OR gate	Dual 2-input EXCLUSIVE-OR gate	•	•	•
74AUP2GU04	Buffer/inverter/driver	Dual inverter; unbuffered	•	•	•
74AUP2T1326	Combination gate	Dual supply buffer/line driver; 3-state	•	•	•
74AUP3G04	Buffer/inverter/driver	Triple inverter	•	•	•
74AUP3G0434	Combination gate	Dual inverter and single buffer	•	•	•
74AUP3G3404	Combination gate	Dual buffer and single inverter	•	•	•

AXP LOGIC

As the first logic family fully specified at 0.8 V, the Advanced eXtremely low voltage and Power (AXP) family is a speed upgrade to the 1.8 V AUP family, but without an increase in dynamic power dissipation. These devices are ultra-low-power, small-footprint solutions for use in 1.2 and 1.2/2.5 V applications. Supporting a supply range from 0.75 to 2.75 V, AXP logic supports the trend toward lower-voltage nodes of 1.2 and 0.8 V. All are fully specified from -40 to 85 °C.

Features and benefits

- Very low dynamic power dissipation (C_{PD})
- Wide supply range (0.7 to 2.75 V)
- Fully specified at 0.8 V
- Wide operating temperature (-40 to 85 °C)
- t_{pd} of 4.6 ns and I_O of ±4.5 mA at 1.2 V supply

Applications

- Smartphones, tablets
- Digital cameras
- Portable medical devices
- Other power-sensitive applications

AXP selection table

			MicroPak	MicroPak	MicroPak	MicroPak
Type number	**Function**	**Description**	**Suffix GM**	**Suffix GN**	**Suffix GS**	**Suffix GX**
74AXP1G06	Buffer/inverter/driver	Single inverter; open drain	•	•	•	•
74AXP1G08	AND gate	Single 2-input AND gate	•	•	•	•
74AXP1G125	Buffer/inverter/driver	Single buffer/line driver (3-state)	•	•	•	•
74AXP1G57	Configurable multi-function gate	Configurable gate; Schmitt trigger	•	•	•	
74AXP1G58	Configurable multi-function gate	Configurable gate; Schmitt trigger	•	•	•	
74AXP1G97	Configurable multi-function gate	Configurable gate; Schmitt trigger	•	•	•	•
74AXP1G98	Configurable multi-function gate	Configurable gate; Schmitt trigger	•	•	•	•
74AXP1G00	NAND Gate	single 2-input NAND gate, Low-power 2-input NAND gate	•			•
74AXP1G02	NOR Gate	single 2-input NOR gate, Low-power 2-input NOR gate	•			•
74AXP1G04	Buffer/inverter/driver	single inverter, Low-power inverter	•			•
74AXP1G07	Buffer/inverter/driver	Low Power Buffer with Open Drain Outputs	•			•
74AXP1G09	AND Gate	Low-power 2-input AND gate with open-drain	•			•
74AXP1G10	NAND Gate	Low Power 3-input NAND Gate	•			
74AXP1G11	AND Gate	Low Power 3-input AND Gate	•			
74AXP1G14	Schmitt Triggers	single inverter Schmitt trigger, Low-power Schmitt trigger inverter	•	•	•	•
74AXP1G157	Multiplexer	Single 2-input Multiplexer	•			
74AXP1G17	Schmitt Triggers	Low-power Schmitt trigger, Low-power Schmitt trigger	•			•
74AXP1G32	OR Gates	Single 2-input OR gate, Low-power 2-input OR gate	•			•
74AXP1G86	EX-OR Gate	Low-power 2-input EXCLUSIVE-OR gate	•			•
74AXP2G07	Buffer/inverter/driver	Low-power dual buffer with open-drain output, Low-power dual buffer with open-drain output	•	•	•	•
74AXP2G14	Buffer/inverter/driver	Low-power dual Schmitt trigger inverter, Low-power dual Schmitt Trigger Inverter	•	•	•	•
74AXP2G17	Buffer/inverter/driver	Low-power dual Schmitt trigger	•			
74AXP2G34	Buffer	Low-power dual Buffer	•			
74AXP2G3404	Buffer and Inverter	Low power buffer and inverter	•			

CBTLV(D) LOGIC

CBTLV and CBTLVD bus switches are low-delay, single-transistor or transmission-gate solutions for multiplexing data buses, hot-swapping boards in backplanes, memory interleaving, signal conditioning, or unidirectional level shifting. They are fully specified from either -40 to +85 °C or from -40 to +125 °C.

Features and benefits

- 5-to-3.3 V level shifting
- 3.3-to-1.8 V level shifting
- Low propagation delay
- TTL control inputs

Applications

- Telecommunications infrastructure
- Memory interleaving
- Industrial control
- Unidirectional level shifting
- Cell phones

CBTLV(D) selection table

			TSSOP	SSOP	SO	DQFN	Micro	PicoGate
Type number	Function	Description	Suffix DGG, DGV, PW	Suffix DK, DS	Suffix D	Suffix BQ	Suffix GF, GM, GN, GS	Suffix GV, GW
74CBTLV16211	Bus switch	24-bit bus switch	•					
74CBTLV1G125	Bus switch	Single bus switch					•	•
74CBTLV3125	Bus switch	Quad bus switch	•	•		•		
74CBTLV3126	Bus switch	Quad bus switch	•	•		•		
74CBTLV3244	Bus switch	Octal bus switch	•	•		•		
74CBTLV3245	Bus switch	Octal bus switch	•	•		•		
74CBTLV3253	Mux/demux	Dual 4:1 mux/demux	•	•	•	•		
74CBTLV3257	Mux/demux	Quad 2:1 mux/demux	•	•	•	•		
74CBTLV3384	Bus switch	10-bit bus switch	•	•		•		
74CBTLV3861	Bus switch	10-bit bus switch	•	•		•		
74CBTLVD3244	Bus switch level shifter	Octal bus switch level translator	•	•		•		
74CBTLVD3245	Bus switch level shifter	Octal bus switch level translator	•	•		•		
74CBTLVD3384	Bus switch level shifter	10-bit bus switch level translator	•	•		•		
74CBTLVD3861	Bus switch level shifter	10-bit bus switch level translator	•	•		•		

Product listing by function

ANALOG SWITCHES

Features and benefits

- Reduced signal attenuation for low switching losses
- Reduced THD for high-quality audio switching
- Fewer ADCs with analog sensor multiplexing
- Integrated level shifting
- Low ON resistance, ON flatness
- Low switch leakage
- Wide supply voltage
- Options for low input threshold
- Overvoltage-tolerant options
- High ESD protection per IEC 61000 standard

Applications

- Audio/video source selection
- Analog sensor multiplexing
- GPIO expansion
- Bus isolation
- Sample-and-hold circuits

Analog switches

Type number	Description	V_{CC} (V)	Logic switching levels	R_{ON} (Ω)	R_{ON}(FLAT) (Ω)	f(-3dB) (MHz)	T_{HD} (%)	X_{talk} (dB)	T_{amb} (°C)
74AHC1G66	Single-pole, single-throw analog switch	2.0 to 5.5	CMOS	40	14	280	0.015		-40 to +125
74AHCT1G66	Single-pole, single-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	40	14	280	0.015		-40 to +125
74HC1G66	Single-pole, single-throw analog switch	2.0 to 9.0	CMOS	105	23	200	0.02		-40 to +125
74HCT1G66	Single-pole, single-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	118	23	180	0.04		-40 to +125
74HC2G66	Dual single-pole, single-throw analog switch	2.0 to 9.0	CMOS	105	23	200	0.02	-60	-40 to +125
74HCT2G66	Dual single-pole, single-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	118	23	180	0.04	-60	-40 to +125
74HC4016	Quad single-pole, single-throw analog switch	2.0 to 10.0	CMOS	300	80	160	0.4	-60	-40 to +125
74HCT4016	Quad single-pole, single-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	400	50	150	0.8	-60	-40 to +125
74HC4051	Single-pole, octal-throw analog switch	2.0 to 10.0	CMOS	200	20	180	0.02		-40 to +125
74HCT4051	Single-pole, octal-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	225	20	170	0.04		-40 to +125
74HC4052	Dual single-pole, quad-throw analog switch	2.0 to 10.0	CMOS	200	20	180	0.02	-60	-40 to +125
74HCT4052	Dual single-pole, quad-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	225	20	170	0.04	-60	-40 to +125
74HC4053	Triple single-pole, double-throw analog switch	2.0 to 10.0	CMOS	200	20	170	0.02		-40 to +125
74HCT4053	Triple single-pole, double-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	225	20	160	0.04		-40 to +125
74HC4066	Quad single-pole, single-throw analog switch	2.0 to 10.0	CMOS	105	23	200	0.02	-60	-40 to +125
74HCT4066	Quad single-pole, single-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	118	23	180	0.04	-60	-40 to +125
74HC4067	Single-pole, 16-throw analog switch	2.0 to 10.0	CMOS	200	25	100	0.02		-40 to +125
74HCT4067	Single-pole, 16-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	225	25	90	0.04		-40 to +125
74HC4316	Quad single-pole, single-throw analog switch with translation	2.0 to 10.0	CMOS	300	80	160	0.4	-60	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Analog switches (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	R_{ON} (Ω)	R_{ON}(FLAT) (Ω)	f(-3dB) (MHz)	T_{HD} (%)	X_{talk} (dB)	T_{amb} (°C)
74HCT4316	Quad single-pole, single-throw analog switch with translation; TTL-enabled	4.5 to 5.5	TTL	400	50	150	0.8	-60	-40 to +125
74HC4351	Single-pole, octal-throw analog switch with latch	2.0 to 10.0	CMOS	200	20	180	0.02		-40 to +125
74HCT4351	Single-pole, octal-throw analog switch with latch; TTL-enabled	4.5 to 5.5	TTL	225	20	170	0.04		-40 to +125
74HC4353	Triple single-pole, double-throw analog switch with latch	4.5 to 5.5	TTL	225	20	160	0.04	-60	-40 to +125
74HCT4353	Triple single-pole, double-throw analog switch with latch; TTL-enabled	4.5 to 5.5	TTL	225	20	160	0.04	-60	-40 to +125
74HC4851	Single-pole, octal-throw analog switch	2.0 to 10.0	CMOS	220					-40 to +125
74HCT4851	Single-pole, octal-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	240					-40 to +125
74HC4852	Dual single-pole, quad-throw analog switch; TTL-enabled	2.0 to 10.0	CMOS	220					-40 to +125
74HCT4852	Dual single-pole, quad-throw analog switch; TTL-enabled	4.5 to 5.5	TTL	240					-40 to +125
74LV4051	Single-pole, octal-throw analog switch	1.0 to 6.0	TTL	135	35	200	0.4	-60	-40 to +125
74LV4052	Dual single-pole, quad-throw analog switch	1.0 to 6.0	TTL	125	15	180	0.4	-60	-40 to +125
74LV4053	Triple single-pole, double-throw analog switch	1.0 to 6.0	TTL	150	30	180	0.4	-60	-40 to +125
74LV4066	Quad single-pole, single-throw analog switch	1.0 to 6.0	TTL	50	3	180	0.02	-60	-40 to +125
74LVC1G3157	Single-pole, double-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	300	0.078		-40 to +125
74LVC1G384	Single-pole, single-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	440	0.001		-40 to +125
74LVC1G53	Single-pole, double-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	300	0.078		-40 to +125
74LVC1G66	Single-pole, single-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	440	0.001		-40 to +125
74LVC2G53	Single-pole, double-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	300	0.078		-40 to +125
74LVC2G66	Dual single-pole, single-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	440	0.005		-40 to +125
74LVC4066	Quad single-pole, single-throw analog switch	1.65 to 5.5	CMOS/ LVTTL	15	1,5	440	0.005		-40 to +125
74LVCV2G66	Dual single-pole, single-throw analog switch; overvoltage tolerant	2.3 to 5.5	CMOS/ LVTTL	15	3	210	0.01		-40 to +125
HEF4016	Quad single-pole, single-throw analog switch	4.5 to 15.5	CMOS	350	65	90	0.04	-50	-40 to +85
HEF4051	Single-pole, octal-throw analog switch	4.5 to 15.5	CMOS	175	30	70	0.04	-50	-40 to +85
HEF4052	Dual single-pole, quad-throw analog switch	4.5 to 15.5	CMOS	175	30	70	0.04	-50	-40 to +85
HEF4053	Triple single-pole, double-throw analog switch	4.5 to 15.5	CMOS	175	30	70	0.04	-50	-40 to +85
HEC4066	Quad single-pole, single-throw analog switch	4.5 to 15.5	CMOS	175	20	90	0.04	-50	-40 to +85
HEF4067	Single-pole, 16-throw analog switch	4.5 to 15.5	CMOS	175	20	13	0.04	-50	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

BUFFERS/INVERTERS/DRIVERS

Features and benefits

- Improved current drive and signal levels
- Improved signal integrity in complex layouts
- Widths from one to 32 bits
- Inverting, non-inverting variants
- Mixed 3.3/5 V applications
- Wide range of supply voltages
- Low propagation delay
- Optional TTL inputs, 3-state outputs, overvoltage-tolerant inputs, bus hold

Applications

- STBs
- LCD TVs
- Cell phones
- Industrial monitoring

Buffers-inverters-drivers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74AHC04	Hex inverter	2.0 to 5.5	CMOS	±8	50 pF	3	60	-40 to +125
74AHCT04	Hex inverter; TTL-enabled	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74AHC125	Quad buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3	60	-40 to +125
74AHCT125	Quad buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74AHC126	Quad buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.3	60	-40 to +125
74AHCT126	Quad buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74AHC1G04	Single inverter	2.0 to 5.5	CMOS	±8	50 pF	3.1	60	-40 to +125
74AHCT1G04	Single inverter; TTL-enabled	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
74AHC1G06	Single inverter; open drain	2.0 to 5.5	CMOS	8	50 pF	2.7	60	-40 to +125
74AHCT1G06	Single inverter; open drain; TTL-enabled	4.5 to 5.5	TTL	8	50 pF	3	60	-40 to +125
74AHC1G07	Single buffer; open drain	2.0 to 5.5	CMOS	8	50 pF	2.5	60	-40 to +125
74AHCT1G07	Single buffer; open drain; TTL-enabled	4.5 to 5.5	TTL	8	50 pF	2.8	60	-40 to +125
74AHC1G125	Single buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125
74AHCT1G125	Single buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
74AHC1G126	Single buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125
74AHCT1G126	Single buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
74AHC1G17	Single buffer with Schmitt-trigger inputs	2.0 to 5.5	CMOS	±8	50 pF	3.2	60	-40 to +125
74AHCT1G17	Single buffer with Schmitt-trigger inputs; TTL-enabled	4.5 to 5.5	TTL	±8	50 pF	4.1	60	-40 to +125
74AHC240	Octal inverter/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	2.8	60	-40 to +125
74AHCT240	Octal inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74AHC244	Octal buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.5	60	-40 to +125
74AHCT244	Octal buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.5	60	-40 to +125
74AHC2G125	Dual buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125
74AHCT2G125	Dual buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
74AHC2G126	Dual buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Buffers-inverters-drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74AHCT2G126	Dual buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
74AHC2G241	Dual buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125
74AHCT2G241	Dual buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
74AHC3G04	Triple inverter	2.0 to 5.5	CMOS	±8	50 pF	3.1	60	-40 to +125
74AHCT3G04	Triple inverter; TTL-enabled	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74AHC541	Octal buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.5	60	-40 to +125
74AHCT541	Octal buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.5	60	-40 to +125
74AHC1GU04	Single inverter; unbuffered	2.0 to 5.5	CMOS	±8	50 pF	2.6	60	-40 to +125
74AHC3GU04	Triple inverter; unbuffered	2.0 to 5.5	CMOS	±8	50 pF	2.5	60	-40 to +125
74AHCU04	Hex inverter; unbuffered	2.0 to 5.5	CMOS	±8	50 pF	2.4	60	-40 to +125
74ALVC16244	16-bit buffer/line driver (3-state)	1.2 to 3.6	LVTTL	±24	50 pF	1.9	150	-40 to +85
74ALVCH16244	16-bit buffer/line driver with bus hold (3-state)	1.2 to 3.6	LVTTL	±24	30 pF	1.9	150	-40 to +85
74ALVC04	Hex inverter	1.65 to 3.6	LVTTL	±24	30 pF	2	150	-40 to +85
74ALVC125	Quad buffer/line driver (3-state)	1.65 to 3.6	LVTTL	±24	30 pF	1.8	145	-40 to +85
74ALVC244	Octal buffer/line driver (3-state)	1.65 to 3.6	LVTTL	±24	30 pF	2.9	130	-40 to +85
74ALVC541	Octal buffer/line driver (3-state)	1.65 to 3.6	LVTTL	±24	30 pF	2.3	130	-40 to +85
74ALVCH162244	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	LVTTL	±12	30 pF	2.7	150	-40 to +85
74ALVCH162827	20-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	LVTTL	±12	30 pF	2.9	150	-40 to +85
74ALVCH16825	18-bit buffer/line driver with bus hold (3-state)	2.3 to 3.6	LVTTL	±24	30 pF	2	150	-40 to +85
74ALVCH16827	20-bit buffer/line driver with bus hold (3-state)	2.3 to 3.6	LVTTL	±24	30 pF	2	150	-40 to +85
74ALVT162240	16-bit inverter/line driver with bus hold and 30 Ω termination (3-state)	2.3 to 3.6	LVTTL	±12	50 pF	2.6	75	-40 to +85
74ALVT162241	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	LVTTL	±12	50 pF	2.2	75	-40 to +85
74ALVT162244	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	LVTTL	±12	50 pF	2.2	75	-40 to +85
74ALVT16240	16-bit inverter/line driver with bus hold (3-state)	2.3 to 3.6	LVTTL	-32 / +64	50 pF	1.7	200	-40 to +85
74ALVT16241	16-bit buffer/line driver with bus hold (3-state)	2.3 to 3.6	LVTTL	-32 / +64	50 pF	1.3	200	-40 to +85
74ALVT16244	16-bit buffer/line driver with bus hold (3-state)	2.3 to 3.6	LVTTL	-32 / +64	50 pF	1.5	200	-40 to +85
74ALVT162827	20-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	LVTTL	±12	50 pF	2.2	75	-40 to +85
74ALVT16827	20-bit buffer/line driver with bus hold (3-state)	2.3 to 3.6	LVTTL	-32 / +64	50 pF	1.3	200	-40 to +85
74AUP1G04	Single inverter	1.1 to 3.6	CMOS	±1.9	30 pF	4	70	-40 to +125
74AUP1G06	Single inverter; open drain	1.1 to 3.6	CMOS	1,9	30 pF	4.5	70	-40 to +125
74AUP1G07	Single buffer; open drain	1.1 to 3.6	CMOS	1,9	30 pF	4.4	70	-40 to +125
74AUP1G125	Single buffer/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.3	70	-40 to +125
74AUP1G126	Single buffer/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.3	70	-40 to +125
74AUP1G14	Single inverter; Schmitt trigger	1.1 to 3.6	CMOS	±1.9	30 pF	4.7	70	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Buffers-inverters-drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74AUP1G240	Single inverter/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.2	70	-40 to +125
74AUP1G34	Single buffer	1.1 to 3.6	CMOS	±1.9	30 pF	3.9	70	-40 to +125
74AUP1GU04	Single inverter; unbuffered	1.1 to 3.6	CMOS	±1.9	30 pF	2.3	70	-40 to +125
74AUP2G04	Dual inverter	1.1 to 3.6	CMOS	±1.9	30 pF	4	70	-40 to +125
74AUP2G06	Dual inverter; open drain	1.1 to 3.6	CMOS	1,9	30 pF	4.5	70	-40 to +125
74AUP2G07	Dual buffer; open drain	1.1 to 3.6	CMOS	1,9	30 pF	4.4	70	-40 to +125
74AUP2G125	Dual buffer/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.3	70	-40 to +125
74AUP2G126	Dual buffer/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.3	70	-40 to +125
74AUP2G14	Dual inverter; Schmitt trigger	1.1 to 3.6	CMOS	±1.9	30 pF	4.7	70	-40 to +125
74AUP2G240	Dual inverter/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.2	70	-40 to +125
74AUP2G241	Dual buffer/line driver (3-state)	1.1 to 3.6	CMOS	±1.9	30 pF	4.3	70	-40 to +125
74AUP2G34	Dual buffer	1.1 to 3.6	CMOS	±1.9	30 pF	3.9	70	-40 to +125
74AUP2GU04	Dual inverter; unbuffered	1.1 to 3.6	CMOS	±1.9	30 pF	2.3	70	-40 to +125
74AUP3G04	Triple inverter	1.1 to 3.6	CMOS	±1.9	30 pF	4	70	-40 to +125
74AVC16244	16-bit buffer/line driver (3-state)	0.8 to 3.6	CMOS/ LVTTL	±12	30 pF	2	200	-40 to +85
74AVCH16244	16-bit buffer/line driver with bus hold (3-state)	0.8 to 3.6	CMOS/ LVTTL	±12	30 pF	2	200	-40 to +85
74AXP1G06	Single inverter; open drain	0.7 to 2.75	CMOS	4,5	5pF	3.5	70	-40 to +85
74AXP1G125	Single buffer/line driver (3-state)	0.7 to 2.75	CMOS	±4.5	5pF	2.7	70	-40 to +85
74HC04	Hex inverter	2.0 to 6.0	CMOS	±5.2	50 pF	7	36	-40 to +125
74HCT04	Hex inverter; TTL-enabled	4.5 to 5.5	TTL	±4.0	50 pF	8	36	-40 to +125
74HC125	Quad buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT125	Quad buffer/line driver (3-state)	4.5 to 5.5	TTL	±6	50 pF	12	36	-40 to +125
74HC126	Quad buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT126	Quad buffer/line driver (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC1G04	Single inverter	2.0 to 6.0	CMOS	±2.6	50 pF	7	36	-40 to +125
74HCT1G04	Single inverter; TTL-enabled	4.5 to 5.5	TTL	±2.0	50 pF	8	36	-40 to +125
74HC1G125	Single buffer/line driver (3-state)	2.0 to 6.0	CMOS	±2.6	50 pF	9	36	-40 to +125
74HCT1G125	Single buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±2.0	50 pF	10	36	-40 to +125
74HC1G126	Single buffer/line driver (3-state)	2.0 to 6.0	CMOS	±2.6	50 pF	9	36	-40 to +125
74HCT1G126	Single buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±2.0	50 pF	10	36	-40 to +125
74HC240	Octal inverter/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT240	Octal inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	9	36	-40 to +125
74HCT240	Octal inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	9	36	-40 to +125
74HCT240	Octal inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	9	36	-40 to +125
74HC241	Octal buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	7	36	-40 to +125
74HCT241	Octal buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Buffers-inverters-drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74HC244	Octal buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT244	Octal buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC2G04	Dual inverter	2.0 to 6.0	CMOS	±5.2	50 pF	8	36	-40 to +125
74HCT2G04	Dual inverter; TTL-enabled	4.5 to 5.5	TTL	±4.0	50 pF	10	36	-40 to +125
74HC2G125	Dual buffer/line driver (3-state)	2.0 to 6.0	CMOS	±5.2	50 pF	10	36	-40 to +125
74HCT2G125	Dual buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±4.0	50 pF	12	36	-40 to +125
74HC2G126	Dual buffer/line driver (3-state)	2.0 to 6.0	CMOS	±5.2	50 pF	10	36	-40 to +125
74HC2G34	Dual buffer	2.0 to 6.0	CMOS	±5.2	50 pF	9	36	-40 to +125
74HCT2G34	Dual buffer; TTL-enabled	4.5 to 5.5	TTL	±4	50 pF	10	32	-40 to +125
74HC365	Hex buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT365	Hex buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC366	Hex inverter/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	10	36	-40 to +125
74HCT366	Hex inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC367	Hex buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	8	36	-40 to +125
74HCT367	Hex buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC368	Hex inverter/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT368	Hex inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC3G04	Triple inverter	2.0 to 6.0	CMOS	±5.2	50 pF	8	36	-40 to +125
74HCT3G04	Triple inverter; TTL-enabled	4.5 to 5.5	TTL	±4.0	50 pF	10	36	-40 to +125
74HC3G06	Triple inverter; open drain	2.0 to 6.0	CMOS	5,2	50 pF	9	36	-40 to +125
74HCT3G06	Triple inverter; open drain; TTL-enabled	4.5 to 5.5	TTL	4	50 pF	9	36	-40 to +125
74HC3G07	Triple buffer; open drain	2.0 to 6.0	CMOS	5,2	50 pF	9	36	-40 to +125
74HCT3G07	Triple buffer; open drain; TTL-enabled	4.5 to 5.5	TTL	4	50 pF	9	36	-40 to +125
74HC3G34	Triple buffer	2.0 to 6.0	CMOS	±5.2	50 pF	9	36	-40 to +125
74HCT3G34	Triple buffer; TTL-enabled	4.5 to 5.5	TTL	±4.0	50 pF	10	36	-40 to +125
74HC540	Octal inverter/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	9	36	-40 to +125
74HCT540	Octal inverter/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	11	36	-40 to +125
74HC541	Octal buffer/line driver (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	10	36	-40 to +125
74HCT541	Octal buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	12	36	-40 to +125
74HC05	Hex inverter; open drain	2.0 to 6.0	CMOS	5,2	50 pF	11	36	-40 to +125
74HC1GU04	Single inverter; unbuffered	2.0 to 6.0	CMOS	±2.6	50 pF	5	36	-40 to +125
74HC2GU04	Single inverter; unbuffered	2.0 to 6.0	CMOS	±2.6	50 pF	5	36	-40 to +125
74HC3GU04	Triple inverter; unbuffered	2.0 to 6.0	CMOS	±5.2	50 pF	6	36	-40 to +125
74HC3GU04	Triple inverter; unbuffered	2.0 to 6.0	CMOS	±5.2	50 pF	6	36	-40 to +125
74HCU04	Hex inverter; unbuffered	2.0 to 6.0	CMOS	±5.2	50 pF	5	36	-40 to +125
74LV04	Hex inverter	1.0 to 5.5	CMOS	±12	50 pF	6	30	-40 to +125
74LV125	Quad buffer/line driver (3-state)	1.0 to 5.5	CMOS	±16	50 pF	9	30	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Buffers-inverters-drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74LV241	Octal buffer/line driver (3-state)	1.0 to 5.5	CMOS	±8	50 pF	8	30	-40 to +125
74LV244	Octal buffer/line driver (3-state)	1.0 to 5.5	CMOS	±16	50 pF	8	30	-40 to +125
74LV365	Hex buffer/line driver (3-state)	1.0 to 3.6	CMOS	±8	50 pF	9	30	-40 to +125
74LV367	Hex buffer/line driver (3-state)	1.0 to 3.6	CMOS	±8	50 pF	8	30	-40 to +125
74LV541	Octal buffer/line driver (3-state)	1.0 to 3.6	CMOS	±8	50 pF	10	30	-40 to +125
74LVC162244	16-bit buffer/line driver with 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.9	175	-40 to +125
74LVCH162244	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	50 pF	2.9	175	-40 to +125
74LVC16244	16-bit buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	3	175	-40 to +125
74LVCH16244	16-bit buffer/line driver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	3	175	-40 to +125
74LVC244	Octal buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.8	175	-40 to +125
74LVCH244	Octal buffer/line driver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.8	175	-40 to +125
74LVC04	Hex inverter	1.65 to 5.5	CMOS/ LVTTL	±24	50 pF	2	175	-40 to +125
74LVC06	Hex inverter; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.2	175	-40 to +125
74LVC07	Hex buffer; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.2	175	-40 to +125
74LVC125	Quad buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.4	175	-40 to +125
74LVC126	Quad buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.4	175	-40 to +125
74LVC16240	16-bit inverter/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.7	175	-40 to +125
74LVC16241	16-bit buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.9	175	-40 to +125
74LVC1G04	Single inverter	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2	175	-40 to +125
74LVC1G06	Single inverter; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.3	175	-40 to +125
74LVC1G07	Single buffer; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.2	175	-40 to +125
74LVC1G125	Single buffer/line driver; TTL-enabled (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.1	175	-40 to +125
74LVC1G126	Single buffer/line driver; TTL-enabled (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2	175	-40 to +125
74LVC1G34	Single buffer	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2	175	-40 to +125
74LVC1GU04	Single inverter; unbuffered	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	1.6	175	-40 to +125
74LVC2244	Octal buffer/line driver with 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	50 pF	3.1	175	-40 to +125
74LVC240	Octal inverter/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	3.5	175	-40 to +125
74LVC241	Octal buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	3.2	175	-40 to +125
74LVC2G04	Dual inverter	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.7	175	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Buffers-inverters-drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74LVC2G06	Dual inverter; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.3	175	-40 to +125
74LVC2G07	Dual buffer; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.6	175	-40 to +125
74LVC2G125	Dual buffer/line driver; TTL-enabled (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.3	175	-40 to +125
74LVC2G126	Dual buffer/line driver; TTL-enabled (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.4	175	-40 to +125
74LVC2G240	Dual inverter/line driver (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.5	175	-40 to +125
74LVC2G241	Dual buffer/line driver (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.6	175	-40 to +125
74LVC2G34	Dual buffer	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.2	175	-40 to +125
74LVC2GU04	Dual inverter; unbuffered	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.3	175	-40 to +125
74LVC3G04	Triple inverter	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.7	175	-40 to +125
74LVC3G06	Triple inverter; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2	175	-40 to +125
74LVC3G07	Triple buffer; open drain	1.65 to 5.5	CMOS/ LVTTL	32	50 pF	2.1	175	-40 to +125
74LVC3G34	Triple buffer	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.2	175	-40 to +125
74LVC3GU04	Triple inverter; unbuffered	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2.3	175	-40 to +125
74LVC541	Octal buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	3.3	175	-40 to +125
74LVC827	10-bit buffer/line driver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	4	175	-40 to +125
74LVCH16541	16-bit buffer/line driver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2.7	175	-40 to +125
74LVCH322244	32-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	50 pF	2	175	-40 to +125
74LVCH32244	32-bit buffer/line driver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	3	175	-40 to +125
74LVCU04	Hex inverter; unbuffered	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2	175	-40 to +125
74LVT125	Quad buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.9	150	-40 to +85
74LVTH125	Quad buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.9	150	-40 to +85
74LVT16244	16-bit buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	1.8	150	-40 to +85
74LVTH16244	16-bit buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	1.8	150	-40 to +85
74LVT244	Octal buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.6	150	-40 to +85
74LVTH244	Octal buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.6	150	-40 to +85
74LVT244	Octal buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2	150	-40 to +85
74LVTH244	Octal buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2	150	-40 to +85
74LVT04	Hex inverter	2.7 to 3.6	TTL	-20 / +32	50 pF	2.6	150	-40 to +85
74LVT126	Quad buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.4	150	-40 to +85
74LVT162240	16-bit inverter/line driver with bus hold and 30 Ω termination (3-state)	2.7 to 3.6	TTL	±12	50 pF	2.6	150	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Buffers-inverters-drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load $C_{L\ (Typ)}$	t_{pd} (ns)	f_{max} (MHz)	T_{amb} (°C)
74LVT162244	16-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	50 pF	2.8	150	-40 to +85
74LVT16240	16-bit inverter/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2	150	-40 to +85
74LVT2241	Octal buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	50 pF	3.3	150	-40 to +85
74LVT2244	Octal buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	50 pF	2.9	150	-40 to +85
74LVT240	Octal inverter/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.5	150	-40 to +85
74LVT241	Octal buffer/line driver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	2.8	150	-40 to +85
74LVTN16244	16-bit buffer/line driver (3-state)	2.7 to 3.6	TTL	-32 / +64	50 pF	1.8	150	-40 to +85
74LVU04	Hex inverter; unbuffered	1.0 to 5.5	CMOS	-12 / +12	50 pF	6	30	-40 to +125
74VHC125	Quad buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3	60	-40 to +125
74VHCT125	Quad buffer/line driver (3-state)	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74VHC126	Quad buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.3	60	-40 to +125
74VHCT126	Quad buffer/line driver (3-state)	4.5 to 5.5	TTL	±8	50 pF	3	60	-40 to +125
74VHC244	Octal inverter/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.5	60	-40 to +125
74VHCT244	Octal inverter/line driver (3-state)	4.5 to 5.5	TTL	±8	50 pF	5	60	-40 to +125
74VHC541	Octal buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.5	60	-40 to +125
74VHCT541	Octal buffer/line driver (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.5	60	-40 to +125
HEF40098	Hex inverter	3.0 to 15.0	CMOS	-10 / +20	50 pF	25	10	-40 to +125
HEF40240	Octal inverter/line driver (3-state)	3.0 to 15.0	CMOS	-50 / +45	50 pF	30	10	-40 to +125
HEF40244	Octal buffer/line driver (3-state)	3.0 to 15.0	CMOS	-62 / +45	50 pF	30	10	-40 to +125
HEF4049	Hex inverter/line driver	3.0 to 15.0	CMOS	-3 / +20	50 pF	20	10	-40 to +125
HEF4050	Hex buffer/line driver	3.0 to 15.0	CMOS	-3 / +20	50 pF	40	10	-40 to +125
HEF4069	Hex inverter; unbuffered	3.0 to 15.0	CMOS	±3.4	50 pF	15	10	-40 to +125
XC7SET04	Single inverter; TTL-enabled	4.5 to 5.5	TTL	±8	50 pF	3.5	60	-40 to +125
XC7SET125	Single buffer/line driver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.4	60	-40 to +125
XC7SH04	Single inverter	2.0 to 5.5	CMOS	±8	50 pF	3.5	60	-40 to +125
XC7SH125	Single buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125
XC7SHU04	Single inverter; unbuffered	2.0 to 5.5	CMOS	±8	50 pF	3.5	60	-40 to +125
XC7WH126	Dual buffer/line driver (3-state)	2.0 to 5.5	CMOS	±8	50 pF	3.4	60	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

BUS SWITCHES

Features and benefits

- Level shifting (1.8/3.3 or 3.3/5 V)
- Low propagation delay
- TTL control inputs

Applications

- Telecommunications infrastructure
- Industrial control
- Cell phones
- Unidirectional level shifting
- Backplane hotswap
- Memory interleaving
- Signal conditioning

Bus switches

Type number	Description	V_{CC} (V)	V_{PASS} (V)	Logic switching levels	R_{ON} (Ω)	f(-3dB) (MHz)	Number of bits	t_{pd} (ns)	T_{amb} (°C)
74CBTLV16211	24-bit bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	10	0.2	-40 to +125
74CBTLV1G125	Single bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	1	0.2	-40 to +125
74CBTLV3125	Quad bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	4	0.2	-40 to +125
74CBTLV3126	Quad bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	4	0.2	-40 to +125
74CBTLV3244	Octal bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	8	0.2	-40 to +125
74CBTLV3245	Octal bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	8	0.2	-40 to +125
74CBTLV3253	Dual 4:1 mux/demux	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	2	0.2	-40 to +125
74CBTLV3257	Quad 2:1 mux/demux	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	4	0.2	-40 to +125
74CBTLV3384	10-bit bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	10	0.2	-40 to +125
74CBTLV3861	10-bit bus switch	2.3 to 3.6	3,3	CMOS / LVTTL	7	400	10	0.2	-40 to +125
74CBTLVD3244	Octal bus switch level translator	3.0 to 3.6	1,8	CMOS / LVTTL	7	400	8	0.2	-40 to +125
74CBTLVD3245	Octal bus switch level translator	3.0 to 3.6	1,8	CMOS / LVTTL	7	400	8	0.2	-40 to +125
74CBTLVD3384	10-bit bus switch level translator	3.0 to 3.6	1,8	CMOS / LVTTL	7	400	10	0.2	-40 to +125
74CBTLVD3861	10-bit bus switch level translator	3.0 to 3.6	1,8	CMOS / LVTTL	7	400	10	0.2	-40 to +125
CBT16210	20-bit bus switch	4.5 to 5.5	3,9	TTL	7	300	20	0.25	-40 to +85
CBT16211	24-bit bus switch	4.5 to 5.5	3,9	TTL	7	300	24	0.25	-40 to +85
CBT16212	24-bit bus exchange switch	4.5 to 5.5	3,9	TTL	7	300	24	0.25	-40 to +85
CBT16292	12-bit 2:1 mux/demux	4.5 to 5.5	3,9	TTL	8	300	12	0.4	-40 to +85
CBT3125	Quad bus switch	4.5 to 5.5	3,9	TTL	7	300	4	0.25	-40 to +85
CBT3126	Quad bus switch	4.5 to 5.5	3,9	TTL	7	300	4	0.25	-40 to +85
CBT3244	Octal bus switch	4.5 to 5.5	3,9	TTL	7	300	8	0.25	-40 to +85
CBT3245	Octal bus switch	4.5 to 5.5	3,9	TTL	7	300	8	0.25	-40 to +85
CBT3251	8:1 mux/demux	4.5 to 5.5	3,9	TTL	7	300	8	0.25	-40 to +85
CBT3253	Dual 4:1 mux/demux	4.5 to 5.5	3,9	TTL	7	300	2	0.25	-40 to +85
CBT3257	Quad 2:1 mux/demux	4.5 to 5.5	3,9	TTL	7	300	4	0.25	-40 to +85
CBT3306	Dual bus switch	4.5 to 5.5	3,9	TTL	7	300	2	0.25	-40 to +85
CBT3384	10-bit bus switch	4.5 to 5.5	3,9	TTL	7	300	10	0.25	-40 to +85
CBT3861	10-bit bus switch	4.5 to 5.5	3,9	TTL	7	300	10	0.25	-40 to +85
CBTD16210	20-bit bus switch level translator	4.5 to 5.5	3,3	TTL	7	300	20	0.25	-40 to +85
CBTD16211	24-bit bus switch level translator	4.5 to 5.5	3,3	TTL	7	300	24	0.25	-40 to +85
CBTD3306	Dual bus switch level translator	4.5 to 5.5	3,3	TTL	7	300	2	0.25	-40 to +85
CBTD3384	10-bit bus switch level translator	4.5 to 5.5	3,3	TTL	7	300	10	0.25	-40 to +85
CBTD3861	10-bit bus switch level translator	4.5 to 5.5	3,3	TTL	7	300	10	0,25	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

COUNTERS/FREQUENCY DIVIDERS

Features and benefits

- Integrated oscillator
- Low-power CMOS
- TTL-compatible inputs

Applications

- Generate clock signals
- Frequency-divide external clock signals
- Initiate events after a pre-set number of clock pulses

Counters/frequency dividers

Type number	Description	V_{CC} (V)	Output drive capability (mA)	Logic switching levels	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74HC160	Presettable synchronous BCD decade counter; asynchronous reset	2.0 to 6.0	±5.2	CMOS	18	50 pF	55	-40 to +125
74HCT160	Presettable synchronous BCD decade counter; asynchronous reset; TTL-enabled	4.5 to 5.5	±4.0	TTL	21	50 pF	28	-40 to +125
74HC161	Presettable synchronous 4-bit binary counter; asynchronous reset	2.0 to 6.0	±5.2	CMOS	19	50 pF	48	-40 to +125
74HCT161	Presettable synchronous 4-bit binary counter; asynchronous reset; TTL-enabled	4.5 to 5.5	±4.0	TTL	20	50 pF	41	-40 to +125
74HC163	Presettable synchronous 4-bit binary counter; synchronous reset	2.0 to 6.0	±5.2	CMOS	17	50 pF	50	-40 to +125
74HCT163	Presettable synchronous 4-bit binary counter; synchronous reset; TTL-enabled	4.5 to 5.5	±4.0	TTL	20	50 pF	50	-40 to +125
74HC191	Presettable synchronous 4-bit binary up/down counter	2.0 to 6.0	±5.2	CMOS	22	50 pF	36	-40 to +125
74HCT191	Presettable synchronous 4-bit binary up/down counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	22	50 pF	39	-40 to +125
74HC193	Presettable synchronous 4-bit binary up/down counter; separate up/down clocks	2.0 to 6.0	±5.2	CMOS	20	50 pF	49	-40 to +125
74HCT193	Presettable synchronous 4-bit binary up/down counter; separate up/down clocks; TTL-enabled	4.5 to 5.5	±4.0	TTL	20	50 pF	43	-40 to +125
74HC390	Dual decade ripple counter	2.0 to 6.0	±5.2	CMOS	14	50 pF	60	-40 to +125
74HCT390	Dual decade ripple counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	18	50 pF	55	-40 to +125
74HC393	Dual 4-bit binary ripple counter	2.0 to 6.0	±5.2	CMOS	12	50 pF	107	-40 to +125
74HCT393	Dual 4-bit binary ripple counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	20	50 pF	53	-40 to +125
74HC4017	Johnson decade counter with 10 decoded outputs	2.0 to 6.0	±5.2	CMOS	18	50 pF	77	-40 to +125
74HCT4017	Johnson decade counter with 10 decoded outputs; TTL-enabled	4.5 to 5.5	±4.0	TTL	21	50 pF	67	-40 to +125
74HC4020	14-stage binary ripple counter	2.0 to 6.0	±5.2	CMOS	11	50 pF	52	-40 to +125
74HCT4020	14-stage binary ripple counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	15	50 pF	52	-40 to +125
74HC4040	12-stage binary ripple counter	2.0 to 6.0	±5.2	CMOS	14	50 pF	90	-40 to +125
74HCT4040	12-stage binary ripple counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	16	50 pF	79	-40 to +125
74HC4059	Programmable divide-by-n counter	2.0 to 6.0	±5.2	CMOS	17	50 pF	43	-40 to +125
74HCT4059	Programmable divide-by-n counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	20	50 pF	40	-40 to +125
74HC4060	14-stage binary ripple counter with oscillator	2.0 to 6.0	±5.2	CMOS	31	50 pF	95	-40 to +125
74HCT4060	14-stage binary ripple counter with oscillator; TTL-enabled	4.5 to 5.5	±4.0	TTL	31	50 pF	88	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Counters/frequency dividers (cont.)

Type number	Description	V_{CC} (V)	Output drive capability (mA)	Logic switching levels	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74HC4520	Dual 4-bit synchronous binary counter	2.0 to 6.0	±5.2	CMOS	24	50 pF	64	-40 to +125
74HCT4520	Dual 4-bit synchronous binary counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	24	50 pF	64	-40 to +125
74HC5555	Programmable delay timer with oscillator	2.0 to 6.0	- 20/ + 25	CMOS	89	50 pF	24	-40 to +125
74HCT5555	Programmable delay timer with oscillator; TTL-enabled	4.5 to 5.5	±20	TTL	75	50 pF	24	-40 to +125
74HC6323	Programmable ripple counter with oscillator (3-state)	2.0 to 6.0	±7.8	CMOS	17	50 pF	100	-40 to +125
74HCT6323	Programmable ripple counter with oscillator (3-state); TTL-enabled	4.5 to 5.5	±4.0	TTL	17	50 pF	85	-40 to +125
74HC93	4-bit binary ripple counter	2.0 to 6.0	±5.2	CMOS	12	50 pF	100	-40 to +125
74HCT93	4-bit binary ripple counter; TTL-enabled	4.5 to 5.5	±4.0	TTL	15	50 pF	77	-40 to +125
74HC40103	8-bit synchronous binary down counter	2.0 to 6.0	±5.2	CMOS	15	50 pF	14	-40 to +125
74HC4024	7-stage binary ripple counter	2.0 to 6.0	±5.2	CMOS	14	50 pF	90	-40 to +125
74HC590	8-bit binary counter with output register (3-state)	2.0 to 6.0	±5.2	CMOS	19	50 pF	61	-40 to +125
74LV393	Dual 4-bit binary ripple counter	1.0 to 3.6	±6	TTL	12	50 pF	90	-40 to +125
74LV4020	14-stage binary ripple counter	1.0 to 5.5	±6	TTL	16	50 pF	100	-40 to +125
74LV4060	14-stage binary ripple counter with oscillator	1.0 to 5.5	±6	TTL	29	50 pF	100	-40 to +125
74LVC161	Presettable synchronous 4-bit binary counter; asynchronous reset	1.2 to 3.6	±24	CMOS/ LVTTL	4.9	50 pF	200	-40 to +125
74LVC163	Presettable synchronous 4-bit binary counter; synchronous reset	1.2 to 3.6	±24	CMOS/ LVTTL	4.9	50 pF	200	-40 to +125
HEF4017	Johnson decade counter with 10 decoded outputs	4.5 to 15	±2.4	CMOS	40	50 pF	30	-40 to +85
HEF40193	Presettable synchronous 4-bit binary up/down counter; separate up/down clocks	4.5 to 15.5	±2.4	CMOS	60	50 pF	18	-40 to +85
HEF4020	14-stage binary ripple counter	4.5 to 15.5	±2.4	CMOS	35	50 pF	35	-40 to +85
HEF4024	7-stage binary ripple counter	4.5 to 15.5	±2.4	CMOS	30	50 pF	35	-40 to +85
HEF4040	12-stage binary ripple counter	4.5 to 15.5	±2.4	CMOS	35	50 pF	50	-40 to +85
HEF4059	Programmable divide-by-n counter	4.5 to 15.5	-7/+20	CMOS	40	50 pF	20	-40 to +85
HEF4060	14-stage binary ripple counter with oscillator	4.5 to 15.5	±2.4	CMOS	50	50 pF	30	-40 to +85
HEF4516	Presettable synchronous 4-bit binary up/down counter	4.5 to 15.5	±2.4	CMOS	45	50 pF	18	-40 to +85
HEF4518	Dual BCD counter	4.5 to 15	±2.4	CMOS	40	50 pF	40	-40 to +85
HEF4520	Dual 4-bit synchronous binary counter	4.5 to 15.5	±2.4	CMOS	15	50 pF	40	-40 to +85
HEF4521	24-stage frequency divider and oscillator	4.5-15.5 V	±2.4	CMOS	220	50 pF	35	-40 to +85
HEF4526	Programmable 4-bit binary down counter	4.5 to 15.5	±2.4	CMOS	50	50 pF	32	-40 to +85
HEF4541	Programmable timer	4.5 to 15.5	- 4/ + 2.7	CMOS	38	50 pF	150	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

DECODERS/DEMULTIPLEXERS

Features and benefits

- Multiple input enable for easy expansion, independent controls
- Integrated input latch for storing decoder-line addresses
- Asynchronous and synchronous load options
- Can be cascaded
- High frequency
- Bus-width reduction
- Optional overvoltage-tolerant inputs, inverting and non-inverting outputs, and 3-stage outputs

Applications

- Selection of memory banks and peripherals
- I/O expansion
- Memory addressing in automotive (display clusters, GPS, keyless entry)

Decoders demultiplexers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	T_{amb} (°C)
74AHC138	3-to-8 line decoder/demultiplexer; inverting	2.0 to 5.5	CMOS	±8	4.4	50 pF	-40 to +125
74AHCT138	3-to-8 line decoder/demultiplexer; inverting; TTL-enabled	4.5 to 5.5	TTL	±8	4.4	50 pF	-40 to +125
74AHC139	Dual 2-to-4 line decoder/demultiplexer	2.0 to 5.5	CMOS	±8	3.9	50 pF	-40 to +125
74AHCT139	Dual 2-to-4 line decoder/demultiplexer; TTL-enabled	4.5 to 5.5	TTL	±8	3.6	50 pF	-40 to +125
74AUP1G18	1-to-2 demultiplexer (3-state)	1.1 to 3.6	CMOS	1.9/-1.9	3.2	30 pF	-40 to +125
74AUP1G19	1-to-2 decoder/demultiplexer	1.1 to 3.6	CMOS	1.9/-1.9	3	30 pF	-40 to +125
74HC138	3-to-8 line decoder/demultiplexer; inverting	2.0 to 6.0	CMOS	±5.2	12	50 pF	-40 to +125
74HCT138	3-to-8 line decoder/demultiplexer; inverting; TTL-enabled	4.5 to 5.5	TTL	±4	19	50 pF	-40 to +125
74HC139	Dual 2-to-4 line decoder/demultiplexer	2.0 to 6.0	CMOS	±5.2	14	50 pF	-40 to +125
74HCT139	Dual 2-to-4 line decoder/demultiplexer; TTL-enabled	4.5 to 5.5	TTL	±4	16	50 pF	-40 to +125
74HC154	4-to-16 line decoder/demultiplexer	2.0 to 6.0	CMOS	±5.2	11	50 pF	-40 to +125
74HCT154	4-to-16 line decoder/demultiplexer; TTL-enabled	4.5 to 5.5	TTL	±4	13	50 pF	-40 to +125
74HC238	3-to-8 decoder/demultiplexer	2.0 to 6.0	CMOS	±5.2	14	50 pF	-40 to +125
74HCT238	3-to-8 decoder/demultiplexer; TTL-enabled	4.5 to 5.5	TTL	±4	18	50 pF	-40 to +125
74HC42	BCD to decimal decoder (1-of-10)	2.0 to 6.0	CMOS	±5.2	17	50 pF	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Decoders demultiplexers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	T_{amb} (°C)
74HCT42	BCD to decimal decoder (1-of-10); TTL-enabled	4.5 to 5.5	TTL	±4	20	50 pF	-40 to +125
74HC4511	BCD to 7-segment latch/decoder/driver with lamp test input	2.0 to 6.0	CMOS	-10	28	50 pF	-40 to +125
74HCT4511	BCD to 7-segment latch/decoder/driver with lamp test input; TTL-enabled	4.5 to 5.5	TTL	-10	28	50 pF	-40 to +125
74HC4514	4-to-16 decoder/demultiplexer with address latches	2.0 to 6.0	CMOS	±5.2	27	50 pF	-40 to +125
74HCT4514	4-to-16 decoder/demultiplexer with address latches; TTL-enabled	4.5 to 5.5	TTL	±4	30	50 pF	-40 to +125
74HC4515	4-to-16 decoder/demultiplexer with address latches; inverting	2.0 to 6.0	CMOS	±5.2	29	50 pF	-40 to +125
74HCT4515	4-to-16 decoder/demultiplexer with address latches; inverting; TTL-enabled	4.5 to 5.5	TTL	±4	30	50 pF	-40 to +125
74HC137	3-to-8 line decoder/demultiplexer with address latches; inverting	2.0 to 6.0	CMOS	±5.2	18	50 pF	-40 to +125
74HC237	3-to-8 decoder/demultiplexer with address latches	2.0 to 6.0	CMOS	±5.2	18	50 pF	-40 to +125
74LV138	3-to-8 line decoder/demultiplexer; inverting	1.0 to 5.5	TTL	±12	12	50 pF	-40 to +125
74LVC138	3-to-8 line decoder/demultiplexer; inverting	1.2 to 3.6	CMOS/ LVTTL	±24	2.7	50 pF	-40 to +125
74LV139	Dual 2-to-4 line decoder/demultiplexer	1.0 to 5.5	TTL	±12	11	50 pF	-40 to +125
74LVC139	Dual 2-to-4 line decoder/demultiplexer	1.2 to 3.6	CMOS/ LVTTL	±24	2.5	50 pF	-40 to +125
74LVC1G18	1-to-2 demultiplexer (3-state)	1.65 to 5.5	CMOS/ LVTTL	±32	2.3	50 pF	-40 to +125
HEF4028	1-of-10 decoder	4.5 to 15	CMOS	±2.4	30	50 pF	-40 to +85
HEF4511	BCD to 7-segment latch/decoder/driver with lamp test input	4.5 to 15	CMOS	-25/2.4	40	50 pF	-40 to +85
HEF4514	4-to-16 decoder/demultiplexer with address latches	4.5 to 15	CMOS	±2.4	65	50 pF	-40 to +85
HEF4543	BCD to 7-segment latch/decoder/driver with phase input	4.5 to 15	CMOS	±2.4	55	50 pF	-40 to +85
HEF4555	Dual 1-to-4 line decoder/demultiplexer	4.5 to 15	CMOS	±2.4	30	50 pF	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

DIGITAL COMPARATORS

Features and benefits

- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating
- Low-power CMOS
- CMOS or TTL inputs

Applications

- Process controllers
- Servo-motor control

Digital comparators

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	Number of bits	T_{amb} (°C)
74HC688	8-bit magnitude comparator	2.0 to 6.0	CMOS	±5.2	17	50 pF	8	-40 to +125
74HCT688	8-bit magnitude comparator; TTL-enabled	4.5 to 5.5	TTL	±4.0	17	50 pF	8	-40 to +125
74HC85	4-bit magnitude comparator	2.0 to 6.0	CMOS	±5.2	23	50 pF	4	-40 to +125
74HCT85	4-bit magnitude comparator; TTL-enabled	4.5 to 5.5	TTL	±4.0	26	50 pF	4	-40 to +125
HEF4585	4-bit magnitude comparator	4.5 to 15.5	CMOS	±2.4	65	50 pF	4	-40 to +85

DIGITAL MULTIPLEXERS

Features and benefits

- Mixed 3.3/5 V applications
- Bus-width reduction
- High noise immunity
- Low power consumption
- Wide range of supply voltages
- Low propagation delay
- Optional overvoltage-tolerant inputs, complementary outputs

Applications

- Power windows, power locks, power mirror control
- Advanced diagnostics and engine control modules
- Industrial control systems
- Decision-making via voltage sensing in portable electronics
- I/O expansion

Digital multiplexers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load CL (Typ)	t_{pd} (ns)	T_{amb} (°C)
74AHC157	Quad 2-input multiplexer	2.0 to 5.5	CMOS	±8	50 pF	3.2	
74AHCT157	Quad 2-input multiplexer; TTL-enabled	4.5 to 5.5	TTL	±8	50 pF	3.2	-40 to +125
74AHC257	Quad 2-input multiplexer (3-state)	2.0 to 5.5	CMOS	±8	50 pF	2.9	-40 to +125
74AHCT257	Quad 2-input multiplexer; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	50 pF	3.7	-40 to +125
74AUP1G157	Single 2-input multiplexer	1.1 to 3.6	CMOS	1.9/-1.9	30 pF	3.2	-40 to +125
74AUP1G158	Single 2-input multiplexer; inverting	1.1 to 3.6	CMOS	1.9/-1.9	30 pF	3.2	-40 to +125
74AUP2G157	Single 2-input multiplexer	1.1 to 3.6	CMOS	1.9/-1.9	30 pF	3.4	-40 to +125
74HC151	8-input multiplexer	2.0 to 6.0	CMOS	±5.2	50 pF	17	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Digital multiplexers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	Output Load CL (Typ)	t_{pd} (ns)	T_{amb} (°C)
74HCT151	8-input multiplexer; TTL-enabled	4.5 to 5.5	TTL	±4	50 pF	19	-40 to +125
74HC153	Dual 4-input multiplexer	2.0 to 6.0	CMOS	±5.2	50 pF	17	-40 to +125
74HCT153	Dual 4-input multiplexer; TTL-enabled	4.5 to 5.5	TTL	±4	50 pF	19	-40 to +125
74HC157	Quad 2-input multiplexer	2.0 to 6.0	CMOS	±5.2	50 pF	11	-40 to +125
74HCT157	Quad 2-input multiplexer; TTL-enabled	4.5 to 5.5	TTL	±4	50 pF	13	-40 to +125
74HC251	8-input multiplexer (3-state)	2.0 to 6.0	CMOS	±5.2	50 pF	18	-40 to +125
74HCT251	8-input multiplexer; TTL-enabled (3-state)	4.5 to 5.5	TTL	±4	50 pF	22	-40 to +125
74HC253	Dual 4-input multiplexer (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	17	-40 to +125
74HCT253	Dual 4-input multiplexer; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	17	-40 to +125
74HC257	Quad 2-input multiplexer (3-state)	2.0 to 6.0	CMOS	±7.8	50 pF	11	-40 to +125
74HCT257	Quad 2-input multiplexer; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	50 pF	13	-40 to +125
74HC158	Quad 2-input multiplexer; inverting	2.0 to 6.0	CMOS	±5.2	50 pF	12	-40 to +125
74LV153	Dual 4-input multiplexer	1.0 to 3.6	TTL	±6	50 pF	14	-40 to +125
74LV251	8-input multiplexer (3-state)	1.0 to 3.6	TTL	±6	50 pF	17	-40 to +125
74LVC157	Quad 2-input multiplexer	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2,5	-40 to +125
74LVC1G157	Single 2-input multiplexer	1.65 to 5.5	CMOS/ LVTTL	±32	50 pF	2,2	-40 to +125
74LVC257	Quad 2-input multiplexer (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	50 pF	2,4	-40 to +125

ENCODERS

Features and benefits

- Encode 10-line decimal to 4-line BCD
- Standard output capability
- Applications
- LED, LCD, incandescent, fluorescent, or gas-discharge displays
- 10-position switch encoding
- Code converters, generators

Encoders

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Number of bits	T_{amb} (°C)	Package name
74HCT147	10-to-4 line priority encoder; TTL-enabled	4.5 to 5.5	TTL	±4	17	10	-40 to +125	SOT109-1

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

FIFO REGISTERS

Features and benefits

- Wide range of supply voltages
- Independent asynchronous and synchronous inputs and outputs
- Cascadable
- Optional TTL inputs, 3-state outputs

Applications

- Data buffers

FIFO registers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74HC40105	4-bit x 16-word FIFO register	2.0 to 6.0	CMOS	Low	15	50 pF	30	-40 to +125
74HCT40105	4-bit x 16-word FIFO register; TTL-enabled	4.5 to 5.5	TTL	±4 mA	18	50 pF	28	-40 to +125
74HC7030	9-bit x 64-word FIFO register (3-state)	2.0 to 6.0	CMOS	±5.2 mA	36	50 pF	33	-40 to +125
74HCT7030	9-bit x 64-word FIFO register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±4 mA	26	50 pF	29	-40 to +125
74HC7403	4-bit x 16-word FIFO register (3-state)	2.0 to 6.0	CMOS	±5.2 mA	15	50 pF	30	-40 to +125
74HCT7403	4-bit x 16-word FIFO register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8 mA	17	50 pF	30	-40 to +125

FLIP-FLOPS

Features and benefits

- Mixed 3.3/5 V applications
- Improved signal integrity with integrated termination resistors
- Flow-through pinout for easy layout
- Wide range of supply voltage
- Low propagation delay
- Optional overvoltage-tolerant inputs, integrated source-termination resistors, bus hold

Applications

- Frequency division
- Controlled delays
- Interface between asynchronous and synchronous systems

Flip-flops

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74AHC1G79	Single D-type flip-flop; positive-edge trigger	2.0 to 5.5	CMOS	±8	3,5	50 pF	90	-40 to +125
74AHCT1G79	Single D-type flip-flop; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±8	3,5	50 pF	90	-40 to +125
74AHC273	Octal D-type flip-flop with reset; positive-edge trigger	2.0 to 5.5	CMOS	±8	4,2	50 pF	165	-40 to +125
74AHCT273	Octal D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4	50 pF	120	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Flip-flops (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74AHC374	Octal D-type flip-flop; positive-edge trigger (3-state)	2.0 to 5.5	CMOS	±8	4,4	50 pF	185	-40 to +125
74AHCT374	Octal D-type flip-flop; positive-edge trigger (3-state)	4.5 to 5.5	TTL	±8	4,3	50 pF	140	-40 to +125
74AHC377	Octal D-type flip-flop with data enable; positive-edge trigger	2.0 to 5.5	CMOS	±8	3,9	50 pF	175	-40 to +125
74AHCT377	Octal D-type flip-flop with data enable; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4	50 pF	140	-40 to +125
74AHC574	Octal D-type flip-flop; positive-edge trigger (3-state)	2.0 to 5.5	CMOS	±8	4,4	50 pF	130	-40 to +125
74AHCT574	Octal D-type flip-flop; positive-edge trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	4,4	50 pF	130	-40 to +125
74AHC74	Dual D-type flip-flop with set and reset; positive-edge trigger	2.0 to 5.5	CMOS	±8	3,7	50 pF	170	-40 to +125
74AHCT74	Dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±8	3,3	50 pF	160	-40 to +125
74ALVC374	Octal D-type flip-flop; positive-edge trigger (3-state)	1.65 to 3.6	TTL	±24	2,5	50 pF	300	-40 to +85
74ALVC574	Octal D-type flip-flop; positive-edge trigger (3-state)	1.65 to 3.6	TTL	±24	2,5	50 pF	300	-40 to +85
74ALVC74	Dual D-type flip-flop with set and reset; positive-edge trigger	1.65 to 3.6	TTL	±24	2,3	50 pF	425	-40 to +85
74ALVCH16374	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	1.2 to 3.6	TTL	±24	2,3	50 pF	350	-40 to +85
74ALVCH16821	20-bit D-type flip-flop; positive-edge trigger (3-state)	2.3 to 3.6	TTL	±24	2,5	50 pF	350	-40 to +85
74ALVCH16823	18-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	1.2 to 3.6	TTL	±24	2,1	50 pF	350	-40 to +85
74ALVT162821	20-bit D-type flip-flop; positive-edge trigger (3-state)	2.3 to 3.6	TTL	±12	3,2	50 pF	150	-40 to +85
74ALVT162823	18-bit buffer/line driver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	TTL	±12	3	50 pF	150	-40 to +85
74ALVT16374	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	2.3 to 3.6	TTL	-32/+64	2,3	50 pF	250	-40 to +85
74ALVT16821	20-bit D-type flip-flop; positive-edge trigger (3-state)	2.3 to 3.6	TTL	-32/+64	1,8	50 pF	150	-40 to +85
74ALVT16823	18-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	2.3 to 3.6	TTL	-32/+64	1,9	50 pF	250	-40 to +85
74AUP1G175	Single D flip-flop with reset; positive-edge trigger	1.1 to 3.6	CMOS	±1.9	7,4	30 pF	70	-40 to +125
74AUP1G374	Single D-type flip-flop; positive-edge trigger (3-state)	1.1 to 3.6	CMOS	±1.9	7,9	30 pF	400	-40 to +125
74AUP1G74	Single D-type flip-flop with set and reset; positive-edge trigger	1.1 to 3.6	CMOS	±1.9	9,2	30 pF	400	-40 to +125
74AUP1G79	Single D-type flip-flop; positive-edge trigger	1.1 to 3.6	CMOS	±1.9	9,1	30 pF	400	-40 to +125
74AUP1G80	Single D-type flip-flop; positive-edge trigger	1.1 to 3.6	CMOS	±1.9	9,1	30 pF	400	-40 to +125
74AUP2G79	Dual D-type flip-flop; positive-edge trigger	1.1 to 3.6	CMOS	±1.9	8,5	30 pF	400	-40 to +125
74AUP2G80	Dual D-type flip-flop; positive-edge trigger	1.1 to 3.6	CMOS	±1.9	9,1	30 pF	400	-40 to +125
74AVC16374	16-bit D-type flip-flop; positive-edge trigger (3-state)	1.2 to 3.6	CMOS	±12	1,5	30 pF	350	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Flip-flops (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74HC107	Dual JK-type flip-flop with reset; negative-edge trigger	2.0 to 6.0	CMOS	±5.2	16	50 pF	78	-40 to +125
74HCT107	Dual JK-type flip-flop with reset; negative-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	16	50 pF	73	-40 to +125
74HC109	Dual JK-type flip-flop with set and reset; positive-edge trigger	2.0 to 6.0	CMOS	±5.2	15	50 pF	75	-40 to +125
74HCT109	Dual JK-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	17	50 pF	61	-40 to +125
74HC112	Dual JK-type flip-flop with set and reset; negative-edge trigger	2.0 to 6.0	CMOS	±5.2	15	50 pF	66	-40 to +125
74HCT112	Dual JK-type flip-flop with set and reset; negative-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	19	50 pF	70	-40 to +125
74HC173	Quad D-type flip-flop; positive-edge trigger (3-state)	2.0 to 6.0	CMOS	±7.8	17	50 pF	88	-40 to +125
74HCT173	Quad D-type flip-flop; positive-edge trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	17	50 pF	88	-40 to +125
74HC174	Hex D-type flip-flop with reset; positive-edge trigger	2.0 to 6.0	CMOS	±5.2	17	50 pF	99	-40 to +125
74HCT174	Hex D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	18	50 pF	69	-40 to +125
74HC175	Quad D-type flip-flop with reset; positive-edge trigger	2.0 to 6.0	CMOS	±5.2	17	50 pF	83	-40 to +125
74HCT175	Quad D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	16	50 pF	54	-40 to +125
74HC273	Octal D-type flip-flop with reset; positive-edge trigger	2.0 to 6.0	CMOS	±5.2	15	50 pF	122	-40 to +125
74HCT273	Octal D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	15	50 pF	36	-40 to +125
74HC374	Octal D-type flip-flop; positive-edge trigger (3-state)	2.0 to 6.0	CMOS	±7.8	14	50 pF	83	-40 to +125
74HCT374	Octal D-type flip-flop; positive-edge trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	13	50 pF	48	-40 to +125
74HC377	Octal D-type flip-flop with data enable; positive-edge trigger	2.0 to 6.0	CMOS	±7.8	13	50 pF	83	-40 to +125
74HCT377	Octal D-type flip-flop with data enable; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±6	14	50 pF	53	-40 to +125
74HC574	Octal D-type flip-flop; positive-edge trigger (3-state)	2.0 to 6.0	CMOS	±7.8	14	50 pF	133	-40 to +125
74HCT574	Octal D-type flip-flop; positive-edge trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	15	50 pF	76	-40 to +125
74HC74	Dual D-type flip-flop with set and reset; positive-edge trigger	2.0 to 6.0	CMOS	±5.2	14	50 pF	82	-40 to +125
74HCT74	Dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	4.5 to 5.5	TTL	±4	15	50 pF	59	-40 to +125
74HC73	Dual JK-type flip-flop with reset; negative-edge trigger	2.0 to 6.0	CMOS	±5.2	16	50 pF	77	-40 to +125
74HCT534	Octal D-type flip-flop; inverting; positive-edge trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	13	50 pF	40	-40 to +125
74HCT7273	Octal D-type flip-flop with reset; positive edge-trigger; open drain outputs; TTL-enabled	4.5 to 5.5	TTL	4	16	50 pF	56	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Flip-flops (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74LV174	Hex D-type flip-flop with reset; positive-edge trigger	1.0 to 5.5	TTL	±12	16	50 pF	77	-40 to +125
74LV273	Octal D-type flip-flop with reset; positive-edge trigger	1.0 to 5.5	TTL	±12	12	50 pF	110	-40 to +125
74LV374	Octal D-type flip-flop; positive-edge trigger (3-state)	1.0 to 5.5	TTL	±16	14	50 pF	77	-40 to +125
74LV377	Octal D-type flip-flop with data enable; positive-edge trigger	1.0 to 3.6	TTL	±6	13	50 pF	77	-40 to +125
74LV574	Octal D-type flip-flop; positive-edge trigger (3-state)	1.0 to 5.5	TTL	±16	13	50 pF	77	-40 to +125
74LV74	Dual D-type flip-flop with set and reset; positive-edge trigger	1.0 to 5.5	TTL	±12	11	50 pF	75	-40 to +125
74LVC16374	16-bit D-type flip-flop; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3,8	50 pF	150	-40 to +125
74LVCH16374	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3,8	50 pF	150	-40 to +125
74LVC109	Dual JK-type flip-flop with set and reset; positive-edge trigger	1.2 to 3.6	CMOS/ LVTTL	±24	4	50 pF	330	-40 to +125
74LVC1G175	Single D flip-flop with reset; positive-edge trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3,1	50 pF	300	-40 to +125
74LVC1G74	Single D-type flip-flop with set and reset; positive-edge trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3,5	50 pF	280	-40 to +125
74LVC1G79	Single D-type flip-flop; positive-edge trigger	1.65 to 5.5	CMOS/ LVTTL	±32	2,2	50 pF	450	-40 to +125
74LVC1G80	Single D-type flip-flop; positive-edge trigger	1.65 to 5.5	CMOS/ LVTTL	±32	2,4	50 pF	450	-40 to +125
74LVC273	Octal D-type flip-flop with reset; positive-edge trigger	1.2 to 3.6	CMOS/ LVTTL	±24	6	50 pF	230	-40 to +125
74LVC2G74	Single D-type flip-flop with set and reset; positive-edge trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3,5	50 pF	280	-40 to +125
74LVC374	Octal D-type flip-flop; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	2,7	50 pF	100	-40 to +125
74LVC377	Octal D-type flip-flop with data enable; positive-edge trigger	1.2 to 3.6	CMOS/ LVTTL	±24	6	50 pF	230	-40 to +125
74LVC574	Octal D-type flip-flop; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3,2	50 pF	150	-40 to +125
74LVC74	Dual D-type flip-flop with set and reset; positive-edge trigger	1.2 to 3.6	CMOS/ LVTTL	±24	2,5	50 pF	250	-40 to +125
74LVC821	10-bit D-type flip-flop; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	5,4	50 pF	150	-40 to +125
74LVC823	9-bit D-type flip-flop; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	5,4	50 pF	150	-40 to +125
74LVCH162374	16-bit D-type flip-flop with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3,8	50 pF	150	-40 to +125
74LVCH32374	32-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3,8	50 pF	150	-40 to +125
74LVT16374	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	3	50 pF	150	-40 to +85
74LVTH16374	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	3	50 pF	150	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Flip-flops (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74LVT574	Octal D-type flip-flop; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	4,3	50 pF	150	-40 to +85
74LVTH57	Octal D-type flip-flop; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	4,3	50 pF	150	-40 to +85
74LVTH574	Octal D-type flip-flop; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	4,3	50 pF	150	-40 to +85
74LVT162374	16-bit D-type flip-flop with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	2.7 to 3.6	TTL	±12	3	50 pF	150	-40 to +85
74LVT273	Octal D-type flip-flop with reset; positive-edge trigger	2.7 to 3.6	TTL	-32/+64	3,5	50 pF	150	-40 to +85
74LVT32374	32-bit D-type flip-flop with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	3	50 pF	150	-40 to +85
74LVT373	Octal D-type transparent latch (3-state)	2.7 to 3.6	TTL	-32/+64	3	50 pF		-40 to +85
74LVT374	Octal D-type flip-flop; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	3,5	50 pF	200	-40 to +85
74LVT534	Octal D-type flip-flop; inverting; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32/+64	3,5	50 pF	150	-40 to +85
74LVT74	Dual D-type flip-flop with set and reset; positive-edge trigger	2.7 to 3.6	TTL	-20/+32	3,6	50 pF	345	-40 to +85
HEF4013	Dual D-type flip-flop with set and reset; positive-edge trigger	4.5 to 15.5	CMOS	±2.4	30	50 pF	40	-40 to +85
HEF40174	Hex D-type flip-flop with reset; positive-edge trigger	4.5 to 15.5	CMOS	±2.4	20	50 pF	45	-40 to +85
HEF40175	Quad D-type flip-flop with reset; positive-edge trigger	4.5 to 15.5	CMOS	±2.4	25	50 pF	45	-40 to +85
HEF4027	Dual JK-type flip-flop	4.5 to 15.5	CMOS	±2.4	30	50 pF	30	-40 to +85
HEF40374	Octal D-type flip-flop; positive-edge trigger (3-state)	4.5 to 15.5	CMOS	-50/+62	40	50 pF	17	-40 to +85

FULL ADDERS

Features and benefits

- Cascadable
- Low power dissipation
- Positive or negative logic
- Wide range of supply voltages

Applications

- High-speed 4-bit binary addition

Full adders

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output drive capability (mA)	Number of bits	T_{amb} (°C)
74HC283	4-bit binary full adder with fast carry	2.0 to 6.0	CMOS	±5.2	21	50 pF	4	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

GATES

This section includes AND gates, combination gates (one package, two or more different functions), configurable multi-function gates (one package, nine or more functions), EXCLUSIVE-NOR gates, EXCLUSIVE-OR gates, NOR gates, and OR gates.

Features and benefits

- Mixed 3.3/5 V applications
- Reduced time-to-market for complex designs
- Reduced board space
- Improved signal integrity in complex layouts
- Wide range of supply voltages
- Low propagation delay
- Low-power CMOS
- Optional overvoltage-tolerant inputs, low input threshold
- Comprehensive range: AND, EXCLUSIVE-NOR, EXCLUSIVE-OR, NAND, NOR, OR
- Combination gates and configurable multi-function gates for lower pincount, device count, system cost, assembly-related expenses

Applications

- Control/glue logic
- PCB miniaturization
- Routing simplification
- Discrete replacement

Gates - AND

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AHC08	Quad 2-input AND gate	2.0 to 5.5	CMOS	±8	3.5	50 pF	60	4	-40 to +125
74AHC1G08	Single 2-input AND gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125
74AHC1G09	Single 2-input AND gate; open drain	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125
74AHC2G08	Dual 2-input AND gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	2	-40 to +125
74AHCT08	Quad 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±8	5	50 pF	60	4	-40 to +125
74AHCT1G08	Single 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.6	50 pF	60	1	-40 to +125
74AHCT2G08	Dual 2-Input AND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.6	50 pF	60	2	-40 to +125
74ALVC08	Quad 2-input AND gate	1.65 to 3.6	TTL	±24	2	50 pF	145	4	-40 to +85
74AUP1G08	Single 2-input AND gate	1.1 to 3.6	CMOS	±1.9	8.2	30 pF	70	1	-40 to +125
74AUP1G09	Single 2-input AND gate; open drain	1.1 to 3.6	CMOS	1,9	8.5	30 pF	70	1	-40 to +125
74AUP1G11	Single 3-input AND gate	1.1 to 3.6	CMOS	±1.9	6.9	30 pF	70	1	-40 to +125
74AUP2G08	Dual 2-input AND gate	1.1 to 3.6	CMOS	±1.9	8.2	30 pF	70	2	-40 to +125
74AXP1G08	Single 2-input AND gate	0.7 to 2.75	CMOS	±4.5	2.6	5pF	70	1	-40 to +85
74HC08	Quad 2-input AND gate	2.0 to 6.0	CMOS	±5.2	7	50 pF	36	4	-40 to +125
74HC11	Triple 3-input AND gate	2.0 to 6.0	CMOS	±5.2	10	50 pF	36	3	-40 to +125
74HC1G08	Single 2-input AND gate	2.0 to 6.0	CMOS	±5.2	7	50 pF	36	1	-40 to +125
74HC21	Dual 4-input AND gate	2.0 to 6.0	CMOS	±5.2	10	50 pF	36	2	-40 to +125
74HC2G08	Dual 2-input AND gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	2	-40 to +125
74HCT08	Quad 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±4	11	50 pF	36	4	-40 to +125
74HCT11	Triple 3-input AND gate	4.5 to 5.5	TTL	±4	11	50 pF	36	3	-40 to +125
74HCT1G08	Single 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±2	11	50 pF	36	1	-40 to +125
74HCT1G08	Single 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±2	11	50 pF	36	1	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - AND (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74HCT2G08	Dual 2-Input AND gate; TTL-enabled	4.5 to 5.5	TTL	±4	14	50 pF	36	2	-40 to +125
74LV08	Quad 2-input AND gate	1.0 to 5.5	TTL	±12	7	50 pF	30	4	-40 to +125
74LVC08	Quad 2-input AND gate	1.2 to 3.6	TTL	±24	2.1	50 pF	150	4	-40 to +125
74LVC11	Triple 3-input AND gate	1.2 to 3.6	TTL	±24	3.7	50 pF	150	3	-40 to +125
74LVC1G08	Single 2-input AND gate	1.65 to 5.5	CMOS / LVTTL	±24	2.1	50 pF	150	1	-40 to +125
74LVC1G11	Single 3-input AND gate	1.65 to 5.5	CMOS / LVTTL	±24	2.6	50 pF	150	1	-40 to +125
74LVC2G08	Dual 2-input AND gate	1.65 to 5.5	CMOS / LVTTL	±24	2.1	50 pF	150	2	-40 to +125
74LVT08	Quad 2-input AND gate	2.7 to 3.6	TTL	-32/+64	3.4	50 pF	150	4	-40 to +85
74VHC08	Quad 2-input AND gate	2.0 to 5.5	CMOS	±8	3.5	50 pF	60	4	-40 to +125
74VHCT08	Quad 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±8	5	50 pF	60	4	-40 to +125
HEF4073	Triple 3-input AND gate	4.5 to 15.5	CMOS	±2.4	20	50 pF	10	3	-40 to +85
HEF4081	Quad 2-input AND gate	4.5 to 15.5	CMOS	±2.4	20	50 pF	10	4	-40 to +85
HEF4082	Dual 4-input AND gate	4.5 to 15.5	CMOS	±2.4	25	50 pF	10	2	-40 to +85
XC7SET08	Single 2-input AND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.6	50 pF	60	1	-40 to +125
XC7SH08	Single 2-input AND gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125

Gates - Combination

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AUP1G0832	Single 3-input AND-OR gate	1.1 to 3.6	CMOS	±1.9	6.7	30 pF	70	1	-40 to +125
74AUP1G3208	Single 3-input OR-AND gate	1.1 to 3.6	CMOS	±1.9	7.4	30 pF	70	1	-40 to +125
74AUP1G885	Dual function gate	1.1 to 3.6	CMOS	±1.9	7.6	30 pF	70	1	-40 to +125
74AUP1Z04	Crystal driver with enable and internal resistor	1.1 to 3.6	CMOS	±1.9	5.6	30 pF	70	1	-40 to +125
74AUP1Z125	Crystal driver with enable and internal resistor (3-state)	1.1 to 3.6	CMOS	±1.9	4.7	30 pF	70	1	-40 to +125
74AUP2G0604	Inverter with open drain and inverter	1.1 to 3.6	CMOS	±1.9	4	30 pF	70	2	-40 to +125
74AUP2G3404	Buffer and inverter	1.1 to 3.6	CMOS	±1.9	4	30 pF	70	2	-40 to +125
74AUP2G3407	Buffer and buffer with open drain	1.1 to 3.6	CMOS	±1.9	4.1	30 pF	70	2	-40 to +125
74AUP2T1326	Dual supply buffer/line driver; 3-state	1.1 to 3.6	CMOS	±1.9	3.8	30 pF	70	2	-40 to +125
74AUP3G0434	Dual inverter and single buffer	1.1 to 3.6	CMOS	±1.9	4	30 pF	70	3	-40 to +125
74AUP3G3404	Dual buffer and single inverter	1.1 to 3.6	CMOS	±1.9	4	30 pF	70	3	-40 to +125
74HC58	Dual AND-OR gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	2	-40 to +125
74LVC1GX04	Crystal driver	1.65 to 5.5	CMOS / LVTTL	±24	2.8	50 pF	150	1	-40 to +125
HEF4000	Dual 3-input NOR gate	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	2	-40 to +85
HEF4007	Dual complementary pair and inverter	4.5 to 15.5	CMOS	±3.4	15	50 pF	10	2	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - Configurable

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AUP1G57	Configurable gate; Schmitt trigger	1.1 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AUP1G58	Configurable gate; Schmitt trigger	1.1 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AUP1G97	Configurable gate; Schmitt trigger	1.1 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AUP1G98	Configurable gate; Schmitt trigger	1.1 to 3.6	CMOS	1.9 / -1.9	8.9	30 pF	70	1	-40 to +125
74AUP1T57	Configurable gate with voltage-level translation	2.3 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AUP1T58	Configurable gate with voltage-level translation	2.3 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AUP1T97	Configurable gate with voltage-level translation	2.3 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AUP1T98	Configurable gate with voltage-level translation	2.3 to 3.6	CMOS	1.9 / -1.9	8.7	30 pF	70	1	-40 to +125
74AXP1G57	Configurable gate; Schmitt trigger	0.7 to 2.75	CMOS	4.5 / -4.5	4.6	5pF	70	1	-40 to +85
74AXP1G58	Configurable gate; Schmitt trigger	0.7 to 2.75	CMOS	4.5 / -4.5	4.5	5pF	70	1	-40 to +85
74AXP1G97	Configurable gate; Schmitt trigger	0.7 to 2.75	CMOS	4.5 / -4.5	4.5	5pF	70	1	-40 to +85
74AXP1G98	Configurable gate; Schmitt trigger	0.7 to 2.75	CMOS	4.5 / -4.5	4.5	5pF	70	1	-40 to +85
74LVC1G57	Configurable gate; Schmitt trigger	1.65 to 5.5	TTL	±32	6.3	50 pF	150	1	-40 to +125
74LVC1G58	Configurable gate; Schmitt trigger	1.65 to 5.5	TTL	±32	6.3	50 pF	150	1	-40 to +125
74LVC1G97	Configurable gate; Schmitt trigger	1.65 to 5.5	TTL	±32	6.3	50 pF	150	1	-40 to +125
74LVC1G98	Configurable gate; Schmitt trigger	1.65 to 5.5	TTL	±32	6.3	50 pF	150	1	-40 to +125
74LVC1G99	Configurable gate; Schmitt trigger	1.65 to 5.5	TTL	±32	8.4	50 pF	150	1	-40 to +125

Gates - EXCLUSIVE-NOR

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	T_{amb} (°C)
74HC7266	Quad 2-input EXCLUSIVE-NOR gate	2.0 to 6.0	CMOS	±5.2	11	50 pF	36	-40 to +125
HEF4077	Quad 2-input EXCLUSIVE-NOR gate	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	-40 to +85

Gates - EXCLUSIVE-OR

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AHC1G86	2-input EXCLUSIVE-OR gate	2.0 to 5.5	CMOS	±8	3.4	50 pF	60	1	-40 to +125
74AHCT1G86	2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.5	50 pF	60	1	-40 to +125
74AHC86	Quad 2-input EXCLUSIVE-OR gate	2.0 to 5.5	CMOS	±8	3.4	50 pF	60	4	-40 to +125
74AHCT86	Quad 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.4	50 pF	60	4	-40 to +125
74AUP1G386	Single 3-input EXCLUSIVE-OR gate	1.1 to 3.6	CMOS	1.9/-1.9	8.6	30 pF	70	1	-40 to +125
74AUP2G86	Dual 2-input EXCLUSIVE-OR gate	1.1 to 3.6	CMOS	1.9/-1.9	9	30 pF	70	2	-40 to +125
74HC1G86	Single 2-input EXCLUSIVE-OR gate	2.0 to 6.0	CMOS	±2.6	9	50 pF	36	1	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - EXCLUSIVE-OR (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74HCT1G86	Single 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 to 5.5	TTL	±2.0	10	50 pF	36	1	-40 to +125
74HC2G86	Dual 2-input EXCLUSIVE-OR gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	2	-40 to +125
74HCT2G86	Dual 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 to 5.5	TTL	±4.0	11	50 pF	36	2	-40 to +125
74HC86	Quad 2-input EXCLUSIVE-OR gate	2.0 to 6.0	CMOS	±5.2	11	50 pF	36	4	-40 to +125
74HCT86	Quad 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 to 5.5	TTL	±4	14	50 pF	36	4	-40 to +125
74LV86	Quad 2-input EXCLUSIVE-OR gate	1.0 to 5.5	TTL	±12	11	50 pF	30	4	-40 to +125
74LVC1G386	Single 3-Input EXCLUSIVE-OR gate	1.65 to 5.5	CMOS/ LVTTL	±32	4.5	50 pF	150	1	-40 to +125
74LVC1G86	Single 2-input EXCLUSIVE-OR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.4	50 pF	150	1	-40 to +125
74LVC2G86	Dual 2-input EXCLUSIVE-OR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.3	50 pF	150	2	-40 to +125
74LVC86	Quad 2-input EXCLUSIVE-OR gate	1.2 to 3.6	CMOS/ LVTTL	±24	3	50 pF	150	4	-40 to +125
HEF4030	Quad 2-input EXCLUSIVE-OR gate	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	4	-40 to +85
HEF4070	Quad 2-input EXCLUSIVE-OR gate	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	4	-40 to +85
XC7SET86	2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.5	50 pF	60	1	-40 to +125
XC7SH86	2-input EXCLUSIVE-OR gate	2.0 to 5.5	CMOS	±8	3,4	50 pF	60	1	-40 to +125

Gates - NAND

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AHC00	Quad 2-input NAND gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	4	-40 to +125
74AHCT00	Quad 2-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.3	50 pF	60	4	-40 to +125
74AHC1G00	Single 2-input NAND gate	2.0 to 5.5	CMOS	±8	3.5	50 pF	60	1	-40 to +125
74AHCT1G00	Single 2-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.6	50 pF	60	1	-40 to +125
74AHC2G00	Dual 2-input NAND gate	2.0 to 5.5	CMOS	±8	3.5	50 pF	60	2	-40 to +125
74AHCT2G00	Dual 2-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.6	50 pF	60	2	-40 to +125
74AHC30	8-input NAND gate	2.0 to 5.5	CMOS	±8	3.6	50 pF	60	1	-40 to +125
74AHCT30	8-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.3	50 pF	60	1	-40 to +125
74ALVC00	Quad 2-input NAND gate	1.65-3.6	TTL	±24	2.1	50 pF	145	4	-40 to +85
74AUP1G00	Single 2-input NAND gate	1.1 to 3.6	CMOS	1.9/-1.9	8.3	30 pF	70	1	-40 to +125
74AUP1G132	Single 2-input NAND gate Schmitt trigger	1.1 to 3.6	CMOS	1.9/-1.9	10	30 pF	70	1	-40 to +125
74AUP1G38	Single 2-input NAND gate; open drain	1.1 to 3.6	CMOS	1,9	8.5	30 pF	70	1	-40 to +125
74AUP2G00	Dual 2-input NAND gate	1.1 to 3.6	CMOS	1.9/-1.9	8.3	30 pF	70	2	-40 to +125
74AUP2G38	Dual 2-input NAND gate; open drain	1.1 to 3.6	CMOS	1,9	8.5	30 pF	70	2	-40 to +125
74HC00	Quad 2-input NAND gate	2.0 to 6.0	CMOS	±5.2	7	50 pF	36	4	-40 to +125
74HCT00	Quad 2-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±4	10	50 pF	36	4	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - NAND (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74HC03	Quad 2-input NAND gate; open drain	2.0 to 6.0	CMOS	5,2	8	50 pF	36	4	-40 to +125
74HCT03	Quad 2-input NAND gate; open drain; TTL-enabled	4.5 to 5.5	TTL	±4	10	50 pF	36	4	-40 to +125
74HC10	Triple 3-input NAND gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	3	-40 to +125
74HCT10	Triple 3-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±4	11	50 pF	36	3	-40 to +125
74HC1G00	Single 2-input NAND gate	2.0 to 6.0	CMOS	±2.6	7	50 pF	36	1	-40 to +125
74HCT1G00	Single 2-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±2	10	50 pF	36	1	-40 to +125
74HC20	Dual 4-input NAND gate	2.0 to 6.0	CMOS	±5.2	8	50 pF	36	2	-40 to +125
74HCT20	Dual 4-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±4	13	50 pF	36	2	-40 to +125
74HC2G00	Dual 2-input NAND gate	2.0 to 6.0	CMOS	±5.6	9	50 pF	36	2	-40 to +125
74HCT2G00	Dual 2-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±4	12	50 pF	36	2	-40 to +125
74HC30	8-input NAND gate	2.0 to 6.0	CMOS	±5.2	12	50 pF	36	1	-40 to +125
74HCT30	8-input NAND gate; TTL-enabled	4.5 to 5.5	TTL	±4	12	50 pF	36	1	-40 to +125
74LV00	Quad 2-input NAND gate	1.0 to 5.5	TTL	±12	7	50 pF	30	4	-40 to +125
74LV03	Quad 2-input NAND gate; open drain	1.0 to 5.5	TTL	±12	8	50 pF	30	4	-40 to +125
74LVC00	Quad 2-input NAND gate	1.2 to 3.6	CMOS/ LVTTL	±24	2.1	50 pF	150	4	-40 to +125
74LVC10	Triple 3-input NAND gate	1.2 to 3.6	CMOS/ LVTTL	±24	3.9	50 pF	150	3	-40 to +125
74LVC1G00	Single 2-input NAND gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.2	50 pF	175	1	-40 to +125
74LVC1G10	Single 3-input NAND gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.6	50 pF	175	1	-40 to +125
74LVC1G38	Single 2-input NAND gate; open drain	1.65 to 5.5	CMOS/ LVTTL	32	2.3	50 pF	175	1	-40 to +125
74LVC2G00	Dual 2-input NAND gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.2	50 pF	175	2	-40 to +125
74LVC2G38	Dual 2-input NAND gate; open drain	1.65 to 5.5	CMOS/ LVTTL	32	2.1	50 pF	175	2	-40 to +125
74LVC30	8-input NAND gate	1.65 to 5.6	CMOS/ LVTTL	24	3.6	50 pF	175	1	-40 to +125
74LVC38	Quad 2-input NAND gate; open drain	1.2 to 3.6	CMOS/ LVTTL	24	2.2	50 pF	175	4	-40 to +125
74LVT00	Quad 2-input NAND gate	2.7 to 3.6	TTL	-32/+64	2.7	50 pF	150	4	-40 to +85
74LVT10	Triple 3-input NAND gate	2.7 to 3.6	TTL	-32/+64	3.8	50 pF	150	3	-40 to +85
HEF4011	Quad 2-input NAND gate	4.5 to 15.5	CMOS	±2.4	20	50 pF	10	4	-40 to +85
HEF4023	Triple 3-input NAND gate	4.5 to 15.5	CMOS	±2.4	25	50 pF	10	3	-40 to +85
HEF4068	8-input NAND gate	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	1	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - NOR

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AHCT02	Quad 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.8	50 pF	60	4	-40 to +125
74AHC1G02	Single 2-input NOR gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125
74AHCT1G02	Single 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.5	50 pF	60	1	-40 to +125
74ALVC02	Quad 2-input NOR gate	1.65 to 3.6	TTL	±24	2.2	50 pF	150	4	-40 to +85
74AUP1G02	Single 2-input NOR gate	1.1 to 3.6	CMOS	1.9/-1.9	8.3	30 pF	70	1	-40 to +125
74AUP2G02	Dual 2-input NOR gate	1.1 to 3.6	CMOS	1.9/-1.9	8.3	30 pF	70	2	-40 to +125
74HC02	Quad 2-input NOR gate	2.0 to 6.0	CMOS	±5.2	7	50 pF	36	4	-40 to +125
74HCT02	Quad 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±4	9	50 pF	36	4	-40 to +125
74HC1G02	Single 2-input NOR gate	2.0 to 6.0	CMOS	±2.6	7	50 pF	36	1	-40 to +125
74HCT1G02	Single 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±2.0	9	50 pF	36	1	-40 to +125
74HC27	Triple 3-input NOR gate	2.0 to 6.0	CMOS	±5.2	8	50 pF	36	3	-40 to +125
74HCT27	Triple 3-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±4	10	50 pF	36	3	-40 to +125
74HC2G02	Dual 2-input NOR gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	2	-40 to +125
74HCT2G02	Dual 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±4	12	50 pF	36	2	-40 to +125
74HC4002	Dual 4-input NOR gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	2	-40 to +125
74HCT4002	Dual 4-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±4	11	50 pF	36	2	-40 to +125
74HCT2G02	Dual 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±4	12	50 pF	36	2	-40 to +125
74LV02	Quad 2-input NOR gate	1.0 to 5.5	TTL	±12	6	50 pF	30	4	-40 to +125
74LV27	Triple 3-input NOR gate	1.0 to 5.5	TTL	±12	8	50 pF	30	3	-40 to +125
74LVC02	Quad 2-input NOR gate	1.2 to 3.6	TTL	±24	2.1	50 pF	150	4	-40 to +125
74LVC1G02	Single 2-input NOR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.1	50 pF	150	1	-40 to +125
74LVC1G27	Single 3-input NOR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.6	50 pF	150	1	-40 to +125
74LVC27	Triple 3-input NOR gate	1.2 to 3.6	TTL	±24	3.4	50 pF	150	3	-40 to +125
74LVC2G02	Dual 2-input NOR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.4	50 pF	150	2	-40 to +125
74LVT02	Quad 2-input NOR gate	2.7 to 3.6	TTL	-32/+64	2.8	50 pF		4	-40 to +85
74VHC02	Quad 2-input NOR gate	2.0 to 5.5	CMOS	±8	2.9	50 pF	60	4	-40 to +125
74VHCT02	Quad 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.8	50 pF	60	4	-40 to +125
HEF4001	Quad 2-input NOR gate	4.5 to 15.5	CMOS	±2.4	20	50 pF	10	4	-40 to +85
HEF4002	Dual 4-input NOR gate	4.5 to 15.5	CMOS	±2.4	20	50 pF	10	4	-40 to +85
HEF4025	Triple 3-input NOR gate	4.5 to 15.5	CMOS	±2.4	40	50 pF	10	3	-40 to +85
XC7SET02	Single 2-input NOR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.5	50 pF	60	1	-40 to +125
XC7SH02	Single 2-input NOR gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - OR

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	Power dissipation considerations	T_{amb} (°C)
74AHC1G32	Single 2-input OR gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	low	-40 to +125
74AHCT1G32	Single 2-input OR gate	4.5 to 5.5	TTL	±8	3.3	50 pF	60	1	low	-40 to +125
74AHC2G32	Dual 2-input OR gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	2	low	-40 to +125
74AHCT2G32	Dual 2-input OR gate	4.5 to 5.5	TTL	±8	3.3	50 pF	60	2	low	-40 to +125
74AHC32	Quad 2-input OR gate	2.0 to 5.5	CMOS	±8	3.5	50 pF	60	4	low	-40 to +125
74AHCT32	Quad 2-input OR gate; TTL-enabled	4.5 to 5.5	TTL	±8	5	50 pF	60	4	low	-40 to +125
74ALVC32	Quad 2-input OR gate	1.65 to 3.6	TTL	±24	2	50 pF	150	4	low	-40 to +125
74AUP1G32	Single 2-input OR gate	1.1 to 3.6	CMOS	1.9/-1.9	7.9	30 pF	70	1	ultra low	-40 to +125
74AUP1G332	Single 3-input OR gate	1.1 to 3.6	CMOS	1.9/-1.9	6.8	30 pF	70	1	ultra low	-40 to +125
74AUP2G32	Dual 2-input OR gate	1.1 to 3.6	CMOS	1.9/-1.9	7.9	30 pF	70	2	ultra low	-40 to +125
74HC1G32	Single 2-input OR gate	2.0 to 6.0	CMOS	±2.6	8	50 pF	36	1	low	-40 to +125
74HCT1G32	Single 2-input OR gate; TTL-enabled	4.5 to 5.5	TTL	±2.0	10	50 pF	36	1	low	-40 to +125
74HC2G32	Dual 2-input OR gate	2.0 to 6.0	CMOS	±5.2	9	50 pF	36	2	low	-40 to +125
74HCT2G32	Dual 2-input OR gate; TTL-enabled	4.5 to 5.5	TTL	±4.0	13	50 pF	36	2	low	-40 to +125
74HC32	Quad 2-input OR gate	2.0 to 6.0	CMOS	±5.2	6	50 pF	36	4	low	-40 to +125
74HCT32	Quad 2-input OR gate	4.5 to 5.5	TTL	±4.0	9	50 pF	36	4	low	-40 to +125
74HC4075	Triple 3-input OR gate	2.0 to 6.0	CMOS	±5.2	8	50 pF	36	3	low	-40 to +125
74HCT4075	Triple 3-input OR gate; TTL-enabled	4.5 to 5.5	TTL	±4	10	50 pF	36	3	low	-40 to +125
74LV32	Quad 2-input OR gate	1.0 to 5.5	TTL	±12	6	50 pF	30	4	low	-40 to +125
74LVC1G32	Single 2-input OR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.1	50 pF	150	1	low	-40 to +125
74LVC1G332	Single 3-input OR gate	1.65 to 5.5	CMOS/ LVTTL	±32		50 pF	150	1	low	-40 to +125
74LVC2G32	Dual 2-input OR gate	1.65 to 5.5	CMOS/ LVTTL	±32	2.2	50 pF	150	2	low	-40 to +125
74LVC32	Quad 2-input OR gate	1.2 to 3.6	CMOS/ LVTTL	±24	2.1	50 pF	150	4	low	-40 to +125
74LVC332	Triple 3-input OR gate	1.2 to 3.6	CMOS/ LVTTL	±24	2.4	50 pF	150	3	low	-40 to +125
74LVT32	Quad 2-input OR gate	2.7 to 3.6	TTL	-20/+32	3.2	50 pF		4	medium	-40 to +125
74VHC32	Quad 2-input OR gate	2.0 to 5.5	CMOS	±8	3.5	50 pF	60	4	low	-40 to +125
74VHCT32	Quad 2-input OR gate; TTL-enabled	4.5 to 5.5	TTL	±8	5	50 pF	60	4	low	-40 to +125
HEF4071	Quad 2-input OR gate	4.5 to 15.5	CMOS	±2.4	20	50 pF	10	4	low	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Gates - OR (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	Power dissipation considerations	T_{amb} (°C)
HEF4072	Dual 4-input OR gate	4.5 to 15.5	CMOS	±2.4	25	50 pF	10	2	low	-40 to +85
HEF4075	Triple 3-input OR gate	4.5 to 15.5	CMOS	±2.4	25	50 pF	10	3	low	-40 to +85
XC7SET32	Single 2-input OR gate; TTL-enabled	4.5 to 5.5	TTL	±8	3.3	50 pF	60	1	low	-40 to +125
XC7SH32	Single 2-input OR gate	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	low	-40 to +125

LATCHES / REGISTERED DRIVERS

Features and benefits

- Improved synchronous operation, with reduced signal loads, elimination of timing delays and waveform distortion
- Mixed 3.3/5 V applications
- Reduced board space
- Low-cost interface solutions
- Improved signal integrity in complex layouts
- Wide range of supply voltages
- Low propagation delay
- Low-power CMOS
- Optional overvoltage-tolerant inputs, source termination, low input threshold

Applications

- Memory controllers
- Backplane interfaces

Latches-registered drivers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	Number of bits	T_{amb} (°C)
74AHC259	8-bit addressable latch	2.0 to 5.5	CMOS	±8	4.1	50 pF	8	-40 to +125
74AHCT259	8-bit addressable latch; TTL-enabled	4.5 to 5.5	TTL	±8	4.1	50 pF	8	-40 to +125
74AHC373	Octal D-type transparent latch (3-state)	2.0 to 5.5	CMOS	±8	4.3	50 pF	8	-40 to +125
74AHCT373	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	4.3	50 pF	8	-40 to +125
74AHC573	Octal D-type transparent latch (3-state)	2.0 to 5.5	CMOS	±8	4.2	50 pF	8	-40 to +125
74AHCT573	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	3.9	50 pF	8	-40 to +125
74ALVC162334	16-bit registered driver with 30 Ω termination resistors (3-state)	1.65 to 3.6	LVTTL	±24	6	50 pF	16	-40 to +85
74ALVC162834	18-bit registered driver with 30 Ω termination resistors (3-state)	1.65 to 3.6	LVTTL	±24	6	50 pF	18	-40 to +85
74ALVC162835	18-bit registered driver with 30 Ω termination resistors (3-state)	1.65 to 3.6	LVTTL	±24	6	50 pF	18	-40 to +85
74ALVC162836	20-bit registered driver with 30 Ω termination resistors (3-state)	1.65 to 3.6	LVTTL	±24	6	50 pF	20	-40 to +85
74ALVC16834	18-bit registered driver (3-state)	1.65 to 3.6	LVTTL	±24	4	50 pF	18	-40 to +85
74ALVC16835	18-bit registered driver (3-state)	1.65 to 3.6	LVTTL	±24	4	50 pF	18	-40 to +85
74ALVC16836	20-bit registered driver (3-state)	1.65 to 3.6	LVTTL	±24	4	50 pF	20	-40 to +85
74ALVC373	Octal D-type transparent latch (3-state)	1.65 to 3.6	LVTTL	±24	2.2	50 pF	8	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Latches-registered drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	Number of bits	T_{amb} (°C)
74ALVC573	Octal D-type transparent latch (3-state)	1.65 to 3.6	LVTTL	±24	2.2	50 pF	8	-40 to +85
74ALVCH16373	16-bit D-type transparent latch with bus hold (3-state)	2.3 to 3.6	LVTTL	±24	2.1	50 pF	16	-40 to +85
74ALVCH16832	7-bit to 28-bit address register/driver (3-state)	2.3 to 3.6	LVTTL	±24	4	50 pF	7	-40 to +85
74ALVCH16841	20-bit D-type transparent latch with bus hold (3-state)	2.3 to 3.6	LVTTL	±24	2.4	50 pF	20	-40 to +85
74ALVCH16843	18-bit D-type transparent latch with bus hold (3-state)	2.3 to 3.6	LVTTL	±24	2.1	50 pF	18	-40 to +85
74ALVCH32973	16-bit transceiver and transparent D-type latch with 8 independent buffers	1.8 to 3.6	LVTTL	±24	2.5	50 pF	16	-40 to +85
74ALVT16260	12-bit to 24-bit multiplexed D-type latch with bus hold (3-state)	2.3 to 3.6	TTL	-32 / +64	2.8	50 pF	12	-40 to +85
74ALVT16373	16-bit D-type transparent latch with bus hold (3-state)	2.3 to 3.6	TTL	-32 / +64	1.8	50 pF	16	-40 to +85
74AUP1G373	Single D-type transparent latch (3-state)	1.1 to 3.6	CMOS	1.9 / -1.9	8.5	30 pF	1	-40 to +125
74AVC16334	16-bit registered driver (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	16	-40 to +85
74AVC16373	16-bit D-type transparent latch (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	16	-40 to +85
74AVC16834	18-bit registered driver (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	18	-40 to +85
74AVC16835	18-bit registered driver (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	18	-40 to +85
74AVC16836	20-bit registered driver (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	20	-40 to +85
74AVCM162834	18-bit registered driver with 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	18	-40 to +85
74AVCM162835	18-bit registered driver with 15 Ω termination resistors (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	18	-40 to +85
74AVCM162836	20-bit registered driver with 15 Ω termination resistors (3-state)	1.2 to 3.6	CMOS	±12	2	30 pF	20	-40 to +85
74HC259	8-bit addressable latch	2.0 to 6.0	CMOS	±5.2	18	50 pF	8	-40 to +125
74HCT259	8-bit addressable latch; TTL-enabled	4.5 to 5.5	TTL	±4	20	50 pF	8	-40 to +125
74HC373	Octal D-type transparent latch (3-state)	2.0 to 6.0	CMOS	±7.8	12	50 pF	8	-40 to +125
74HCT373	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	14	50 pF	8	-40 to +125
74HCT563	Octal D-type transparent latch; inverting; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	16	50 pF	8	-40 to +125
74HC573	Octal D-type transparent latch (3-state)	2.0 to 6.0	CMOS	±7.8	14	50 pF	8	-40 to +125
74HCT573	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	17	50 pF	8	-40 to +125
74HC670	4-bit x 4-word register (3-state)	2.0 to 6.0	CMOS	±7.8	17	50 pF	4	-40 to +125
74HCT670	4-bit x 4-word register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	23	50 pF	4	-40 to +125
74HC75	Quad bistable transparent latch	2.0 to 6.0	CMOS	±5.2	11	50 pF	4	-40 to +125
74HC75	Quad bistable transparent latch	2.0 to 6.0	CMOS	±5.2	11	50 pF	4	-40 to +125
74LV259	8-bit addressable latch	1.0 to 3.6	CMOS	±6	17	50 pF	8	-40 to +125
74LV373	Octal D-type transparent latch (3-state)	1.0 to 5.5	CMOS	±16	10	50 pF	8	-40 to +125
74LV573	Octal D-type transparent latch (3-state)	1.0 to 5.5	CMOS	±16	12	50 pF	8	-40 to +125
74LVC162373	16-bit D-type transparent latch with 30 Ω termination resistors (3-state)	1.2 to 3.6	TTL	±12	3.2	50 pF	16	-40 to +125
74LVCH162373	16-bit D-type transparent latch with bus hold and 30 Ω termination resistors (3-state)	1.2 to 3.6	TTL	±24	3.2	50 pF	16	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Latches-registered drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	Number of bits	T_{amb} (°C)
74LVC16373	16-bit D-type transparent latch (3-state)	1.2 to 3.6	TTL	±24	3	50 pF	16	-40 to +125
74LVCH16373	16-bit D-type transparent latch with bus hold (3-state)	1.2 to 3.6	TTL	±24	3	50 pF	16	-40 to +125
74LVC373	Octal D-type transparent latch (3-state)	1.2 to 3.6	TTL	±24	3	50 pF	8	-40 to +125
74LVC573	Octal D-type transparent latch (3-state)	1.2 to 3.6	TTL	±24	3.4	50 pF	8	-40 to +125
74LVC841	10-bit D-type transparent latch (3-state)	1.2 to 3.6	TTL	±24	4.5	50 pF	10	-40 to +125
74LVCH32373	32-bit D-type transparent latch (3-state)	1.2 to 3.6	TTL	±24	3	50 pF	32	-40 to +125
74LVT162373	16-bit D-type transparent latch with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	2.5	50 pF	16	-40 to +85
74LVT16373	16-bit D-type transparent latch with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	50 pF	16	-40 to +85
74LVT573	Octal D-type transparent latch (3-state)	2.7 to 3.6	TTL	-32 / +64	2.7	50 pF	8	-40 to +85
HEF40373	Octal D-type transparent latch (3-state)	4.5 to 15.5	CMOS	-50 / +62	40	50 pF	8	-40 to +85
HEF4043	Quad R/S latch with set and reset (3-state)	4.5 to 15	CMOS	±2.4	25	50 pF	4	-40 to +85
HEF4044	Quad R/S latch with set and reset (3-state)	4.5 to 15	CMOS	±2.4	30	50 pF	4	-40 to +85

LEVEL SHIFTERS/TRANSLATORS

Features and benefits

- Bidirectional operation
- Widths from 1 to 32 bits
- Wide range of supply voltages
- Low propagation delay
- Low-power suspend mode
- Auto-direction sensing
- Optional overvoltage-tolerant inputs, 3-state outputs

Applications

- Mixed-voltage systems
- I^2C bus
- Mobile, portable
- Industrial
- Consumer entertainment
- Computing

Level shifters-translators

Type number	Description	$V_{CC(A)}$ (V)	$V_{CC(B)}$ (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	Number of bits	T_{amb} (°C)
74ALVC164245	16-bit dual-supply voltage-translating transceiver (3-state)	1.5 to 5.5	1.5 to 3.6	CMOS/ LVTTL	±24	2.9	50	16	-40 to +85
74AUP1T34	Single dual-supply translating buffer	1.1 to 3.6	1.1 to 3.6	CMOS	±1.9	15.2	30	1	-40 to +125
74AUP1T45	Single dual-supply voltage-translating transceiver (3-state)	1.1 to 3.6	1.1 to 3.6	CMOS	±1.9	15.6	30	1	-40 to +125
74AVC16T245	16-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	16	-40 to +125
74AVC1T45	Single dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	1	-40 to +125
74AVC20T245	20-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	3.5	30	20	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Level shifters-translators (cont.)

Type number	Description	$V_{CC(A)}$ (V)	$V_{CC(B)}$ (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	Number of bits	T_{amb} (°C)
74AVC2T45	Dual-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	2	-40 to +125
74AVC32T245	32-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	32	-40 to +125
74AVC4T245	4-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	4	-40 to +125
74AVC4TD245	4-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	4	-40 to +125
74AVC8T245	8-bit dual-supply voltage-translating transceiver (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	8	-40 to +125
74AVCH16T245	16-bit dual-supply voltage-translating transceiver with bus hold (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	16	-40 to +125
74AVCH1T45	Single dual-supply voltage-translating transceiver with bus hold (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	1	-40 to +125
74AVCH20T245	20-bit dual-supply voltage-translating transceiver with bus hold (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	3.5	30	20	-40 to +125
74AVCH2T45	Dual-bit dual-supply voltage-translating transceiver with bus hold (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	2	-40 to +125
74AVCH4T245	4-bit dual-supply voltage-translating transceiver with bus hold (3-state)	0.8 to 3.6	0.8 to 3.6	CMOS/ LVTTL	±12	2.1	30	4	-40 to +125
74HC4049	Hex inverter with 15 V-tolerant inputs	2.0 to 6.0	N/A	CMOS	±5.2	8	50	6	-40 to +125
74HC4050	Hex buffer with 15 V-tolerant inputs	2.0 to 6.0	N/A	CMOS	±5.2	7	50	6	-40 to +125
74LVC1T45	Single dual-supply voltage-translating transceiver (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	2.5	50	1	-40 to +125
74LVCH1T45	Single dual-supply voltage-translating transceiver with bus hold (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	2.5	50	1	-40 to +125
74LVC2T45	Dual-bit dual-supply voltage-translating transceiver (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	2.5	50	2	-40 to +125
74LVCH2T45	Dual-bit dual-supply voltage-translating transceiver with bus hold (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	2.5	50	2	-40 to +125
74LVC8T245	8-bit dual-supply voltage-translating transceiver (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	3.5	50	8	-40 to +125
74LVCH8T245	8-bit dual-supply voltage-translating transceiver with bus hold (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	3.5	50	8	-40 to +125
74LVC4245	8-bit dual-supply voltage-translating transceiver (3-state)	1.2 to 5.5	1.2 to 5.5	CMOS/ LVTTL	±24	3.5	50	8	-40 to +125
HEF4104	Quad low-to-high voltage translator (3-state)	3.0 to 15.0	3.0 to 15.0	CMOS	±2.4	340	50	16	-40 to +85
74AXP1T57	Schmitt-trigger inputs, Dual supply configurable multiple function gate	0.7 to 2.75	1.2 to 5.5	1.2 to 5.5	CMOS	±12	4.8	1	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

MULTIVIBRATORS

Features and benefits

- Simple control interface
- Power-on reset
- Dual devices with separate reset inputs
- Negative or positive edge triggered
- Low-power CMOS

Applications

- Timing delays in synchronous control circuits

Multivibrators

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	T_{amb} (°C)
74AHC123	Dual retriggerable monostable multivibrator with reset	2.0 to 5.5	CMOS	±8	5.1	50 pF	-40 to +125
74AHCT123	Dual retriggerable monostable multivibrator with reset; TTL-enabled	4.5 to 5.5	TTL	±8	5	50 pF	-40 to +125
74HC123	Dual retriggerable monostable multivibrator with reset	2.0 to 6.0	CMOS	±7.8	9	50 pF	-40 to +125
74HCT123	Dual retriggerable monostable multivibrator with reset; TTL-enabled	4.5 to 5.5	TTL	±4	26	50 pF	-40 to +125
74HC221	dual non-retriggerable monostable multivibrator with reset	2.0 to 6.0	CMOS	±5.2	29	50 pF	-40 to +125
74HCT221	dual non-retriggerable monostable multivibrator with reset; TTL-enabled	4.5 to 5.5	TTL	±4	32	50 pF	-40 to +125
74HC423	Dual retriggerable monostable multivibrator with reset	2.0 to 6.0	CMOS	±5.2	23	50 pF	-40 to +125
74HCT423	Dual retriggerable monostable multivibrator with reset; TTL-enabled	4.5 to 5.5	TTL	±4	26	50 pF	-40 to +125
74HC4538	Dual retriggerable precision monostable multivibrator	2.0 to 6.0	CMOS	±5.2	27	50 pF	-40 to +125
74HCT4538	Dual retriggerable precision monostable multivibrator; TTL-enabled	4.5 to 5.5	TTL	±4	30	50 pF	-40 to +125
74LV123	Dual retriggerable monostable multivibrator with reset	1.0 to 5.5	TTL	±12	20	50 pF	-40 to +125
74LVC1G123	Single retriggerable monostable multivibrator	1.65 to 5.5	CMOS/ LVTTL	±32	3.5	50 pF	-40 to +125
HEF4047	Monostable/astable multivibrator	4.5 to 15.5	CMOS	±2.4	50	50 pF	-40 to +85
HEF4528	Dual retriggerable monostable multivibrator with reset	4.5 to 15.5	CMOS	±2.4	40	50 pF	-40 to +85

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

PARITY GENERATORS/CHECKERS

Features and benefits

- Simple control interface
- Power-on reset
- Dual devices with separate reset inputs
- Negative or positive edge triggered
- Low-power CMOS

Applications

- Error detection

Parity generators-checkers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	T_{amb} (°C)
74HC280	9-bit odd/even parity generator/checker	2.0 to 6.0	CMOS	±5.2	17	50 pF	-40 to +125
74HCT280	9-bit odd/even parity generator/checker; TTL-enabled	4.5 to 5.5	TTL	±4	18	50 pF	-40 to +125

PHASE-LOCKED LOOPS

Features and benefits

- Phase comparator, loop filter, and VCO
- Wide range of supply voltages
- Maximum frequency to 17 MHz (typ)
- Low power consumption
- Excellent VCO frequency linearity
- Choice of phase comparators
- User configurable

Applications

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Clock recovery
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control interface

Phase-locked loops

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	T_{amb} (°C)
74HC4046	Phase-locked loop with VCO	3.0 to 6.0	CMOS	±5.2	18	50 pF	21
74HCT4046	Phase-locked loop with VCO; TTL-enabled	4.5 to 5.5	TTL	±4	23	50 pF	19
74HC7046	Phase-locked loop with lock detector	3.0 to 6.0	CMOS	±5.2	17	50 pF	19
74HCT7046	Phase-locked loop with lock detector; TTL-enabled	4.5 to 5.5	TTL	±4	21	50 pF	19
74HCT9046	Phase-locked loop with bandgap controlled VCO; TTL-enabled	4.5 to 5.5	TTL	±4	23	50 pF	19
HEF4046	Phase-locked loop with VCO	4.5 to 15.5	CMOS	±2.4		50 pF	2.7

Printer interfaces

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	T_{amb} (°C)
PDI1284P11	Parallel interface transceiver/buffer	3.0 to 3.6	LVTTL	- 14 / 14	13.9	50 pF	0 to +70

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

SCHMITT TRIGGERS

Features and benefits

- Transform slowly changing input signals into sharply defined, jitter-free output signals
- Improve noisy signals
- Reshape signals in complex layouts
- Mixed 3.3/5 V applications
- Wide range of supply voltages
- Input hysteresis
- CMOS and TTL variants
- Optional open-drain outputs, overvoltage-tolerant inputs

Applications

- Convert sine waves to square waves
- Interface between analog and digital environments
- Invoice noise immunity
- Relaxation oscillators

Schmitt triggers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AHC132	Quad 2-input NAND gate Schmitt trigger	2.0 to 5.5	CMOS	±8	3.3	50 pF	60	4	-40 to +125
74AHCT132	Quad 2-input NAND gate Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	3.5	50 pF	60	4	-40 to +125
74AHC14	Hex inverter Schmitt trigger	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	6	-40 to +125
74AHCT14	Hex inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4	50 pF	60	6	-40 to +125
74AHC1G14	Single inverter Schmitt trigger	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125
74AHCT1G14	Single inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4.1	50 pF	60	1	-40 to +125
74AHC3G14	Triple inverter Schmitt trigger	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	3	-40 to +125
74AHCT3G14	Triple inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4.1	50 pF	60	3	-40 to +125
74ALVC14	Hex inverter Schmitt trigger	1.65 to 3.6	TTL	±24	2.4	50 pF	150	6	-40 to +85
74AUP1G17	Single buffer Schmitt trigger	1.1 to 3.6	CMOS	±1.9	7.8	30 pF	70	1	-40 to +125
74AUP2G132	dual 2-input NAND gate Schmitt trigger	1.1 to 3.6	CMOS	±1.9	10	30 pF	70	2	-40 to +125
74AUP2G14	dual inverter Schmitt trigger	1.1 to 3.6	CMOS	±1.9	4.7	30 pF	70	2	-40 to +125
74AUP2G17	dual buffer Schmitt trigger	1.1 to 3.6	CMOS	±1.9	7.8	30 pF	70	2	-40 to +125
74HC132	Quad 2-input NAND gate Schmitt trigger	2.0 to 6.0	CMOS	±5.2	11	50 pF	36	4	-40 to +125
74HCT132	Quad 2-input NAND gate Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±4	17	50 pF	36	4	-40 to +125
74HC14	Hex inverter Schmitt trigger	2.0 to 6.0	CMOS	±5.2	12	50 pF	36	6	-40 to +125
74HCT14	Hex inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±4	17	50 pF	36	6	-40 to +125
74HC1G14	Single inverter Schmitt trigger	2.0 to 6.0	CMOS	±2.6	10	50 pF	36	1	-40 to +125
74HCT1G14	Single inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±2.0	15	50 pF	36	1	-40 to +125
74HC2G14	Dual inverter Schmitt trigger	2.0 to 6.0	CMOS	±5.2	16	50 pF	36	2	-40 to +125
74HCT2G14	Dual inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±4.0	21	50 pF	36	2	-40 to +125
74HC2G17	Dual buffer Schmitt trigger	2.0 to 6.0	CMOS	±5.2	12	50 pF	36	2	-40 to +125
74HCT2G17	Dual buffer Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±4.0	21	50 pF	36	2	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Schmitt triggers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74HC3G14	Triple inverter Schmitt trigger	2.0 to 6.0	CMOS	±5.2	16	50 pF	36	3	-40 to +125
74HCT3G14	Triple inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±4.0	21	50 pF	36	3	-40 to +125
74HC7540	Octal inverter/line driver Schmitt trigger (3-state)	2.0 to 6.0	CMOS	±7.8	11	50 pF	36	8	-40 to +125
74HCT7540	Octal inverter/line driver Schmitt trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	16	50 pF	36	8	-40 to +125
74HC7541	Octal buffer/line driver Schmitt trigger (3-state)	2.0 to 6.0	CMOS	±7.8	11	50 pF	36	8	-40 to +125
74HCT7541	Octal buffer/line driver Schmitt trigger; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	16	50 pF	36	8	-40 to +125
74HC9114	9-bit inverter Schmitt trigger; open drain (3-state)	2.0 to 6.0	CMOS	5,2	12	50 pF	36	9	-40 to +125
74HCT9114	9-bit inverter Schmitt trigger; open drain; TTL-enabled (3-state)	4.5 to 5.5	TTL	4	13	50 pF	36	9	-40 to +125
74HC9115	9-bit buffer Schmitt trigger; open drain (3-state)	2.0 to 6.0	CMOS	5,2	12	50 pF	36	9	-40 to +125
74HCT9115	9-bit buffer Schmitt trigger; open drain; TTL-enabled (3-state)	4.5 to 5.5	TTL	4	13	50 pF	36	9	-40 to +125
74HC7014	Hex buffer precision Schmitt trigger	2.0 to 6.0	CMOS	±5.2	27	50 pF	36	6	-40 to +125
74LV132	Quad 2-input NAND gate Schmitt trigger	1.0 to 5.5	TTL	±12	10	50 pF	30	4	-40 to +125
74LV14	Hex inverter Schmitt trigger	1.0 to 5.5	TTL	±12	13	50 pF	30	6	-40 to +125
74LVC132	Quad 2-input NAND gate Schmitt trigger	1.2 to 3.6	CMOS/ LVTTL	±24	3.4	50 pF	175	4	-40 to +125
74LVC14	Hex inverter Schmitt trigger	1.2 to 3.6	CMOS/ LVTTL	±24	3.2	50 pF	175	6	-40 to +125
74LVC1G14	Single inverter Schmitt trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3	50 pF	175	1	-40 to +125
74LVC1G17	Single buffer Schmitt trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3	50 pF	175	1	-40 to +125
74LVC2G14	Dual inverter Schmitt trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3.9	50 pF	175	2	-40 to +125
74LVC2G17	Dual buffer Schmitt trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3.6	50 pF	175	2	-40 to +125
74LVC3G14	Triple inverter Schmitt trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3.2	50 pF	175	3	-40 to +125
74LVC3G17	Triple buffer Schmitt trigger	1.65 to 5.5	CMOS/ LVTTL	±32	3.6	50 pF	175	3	-40 to +125
74LVT14	Hex inverter Schmitt trigger	2.7 to 3.6	TTL	-32 / +64	3.8	50 pF	150	6	-40 to +125
74VHCT14	Hex inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4.1	50 pF	60	6	-40 to +125
HEF40106	Hex inverter Schmitt trigger	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	6	-40 to +85
HEF4093	Quad 2-input NAND gate Schmitt trigger	4.5 to 15.5	CMOS	±2.4	30	50 pF	10	4	-40 to +125
XC7SET14	Single inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4.1	50 pF	60	1	-40 to +125
XC7SH14	Single inverter Schmitt trigger	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	1	-40 to +125
XC7WH14	Triple inverter Schmitt trigger	2.0 to 5.5	CMOS	±8	3.2	50 pF	60	3	-40 to +125
XC7WT14	Triple inverter Schmitt trigger; TTL-enabled	4.5 to 5.5	TTL	±8	4.1	50 pF	60	3	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

SHIFT REGISTERS/LED DRIVERS

Features and benefits

- Simple control interface
- Asynchronous and synchronous load options
- High frequency
- Cascadable

Applications

- LED displays
- Control units
- I/O expansion

Shift registers - LED drivers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74AHC164	8-bit serial-in/parallel-out shift register	2.0 to 5.5	CMOS	±8	4.5	50 pF	115	8	-40 to +125
74AHCT164	8-bit serial-in/parallel-out shift register; TTL-enabled	4.5 to 5.5	TTL	±8	3.4	50 pF	115	8	-40 to +125
74AHC594	8-bit serial-in/parallel-out shift register with output storage register	2.0 to 5.5	CMOS	±8	4.1	50 pF	160	8	-40 to +125
74AHCT594	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled	4.5 to 5.5	TTL	±8	3.8	50 pF	160	8	-40 to +125
74AHC595	8-bit serial-in/parallel-out shift register with output storage register (3-state)	2.0 to 5.5	CMOS	±8	4	50 pF	170	8	-40 to +125
74AHCT595	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	3.8	50 pF	170	8	-40 to +125
74HC164	8-bit serial-in/parallel-out shift register	2.0 to 6.0	CMOS	±5.2	12	50 pF	78	8	-40 to +125
74HCT164	8-bit serial-in/parallel-out shift register; TTL-enabled	2.0 to 6.0	CMOS	±5.2	12	50 pF	78	8	-40 to +125
74HC165	8-bit parallel or serial-in/serial-out shift register	2.0 to 6.0	CMOS	±5.2	16	50 pF	56	8	-40 to +125
74HCT165	8-bit parallel or serial-in/serial-out shift register; TTL-enabled	4.5 to 5.5	TTL	±4	14	50 pF	48	8	-40 to +125
74HC166	8-bit parallel or serial-in/serial-out shift register	2.0 to 6.0	CMOS	±5.2	15	50 pF	63	8	-40 to +125
74HCT166	8-bit parallel or serial-in/serial-out shift register; TTL-enabled	4.5 to 5.5	TTL	±4.0	23	50 pF	50	8	-40 to +125
74HC194	4-bit bidirectional parallel or serial-in/ parallel-out shift register	2.0 to 6.0	CMOS	±5.2	14	50 pF	102	4	-40 to +125
74HCT194	4-bit bidirectional parallel or serial-in/ parallel-out shift register; TTL-enabled	4.5 to 5.5	TTL	±4	15	50 pF	77	4	-40 to +125
74HC299	8-bit universal shift register (3-state)	2.0 to 6.0	CMOS	±7.8	19	50 pF	54	8	-40 to +125
74HCT299	8-bit universal shift register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	19	50 pF	46	8	-40 to +125
74HC4015	Dual 4-bit serial-in/parallel-out shift register	2.0 to 6.0	CMOS	±5.2	15	50 pF	85	4	-40 to +125
74HCT4015	Dual 4-bit serial-in/parallel-out shift register; TTL-enabled	4.5 to 5.5	TTL	±4	18	50 pF	74	4	-40 to +125
74HC4094	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	2.0 to 6.0	CMOS	±5.2	15	50 pF	95	8	-40 to +125
74HCT4094	8-bit serial-in/serial or parallel-out shift register with output register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±4	19	50 pF	86	8	-40 to +125
74HC594	8-bit serial-in/parallel-out shift register with output storage register	2.0 to 6.0	CMOS	±7.8	14	50 pF	109	8	-40 to +125
74HCT594	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled	4.5 to 5.5	TTL	±6	15	50 pF	100	8	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Shift registers - LED drivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability (mA)	t_{pd} (ns)	Output Load $C_{L\ (Typ)}$	f_{max} (MHz)	Number of bits	T_{amb} (°C)
74HC595	8-bit serial-in/parallel-out shift register with output storage register (3-state)	2.0 to 6.0	CMOS	±7.8	16	50 pF	108	8	-40 to +125
74HCT595	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	25	50 pF	57	8	-40 to +125
74HC597	8-bit parallel or serial-in/parallel-out shift register with parallel input storage register	2.0 to 6.0	CMOS	±5.2	16	50 pF	108	8	-40 to +125
74HCT597	8-bit parallel or serial-in/parallel-out shift register with parallel input storage register; TTL-enabled	4.5 to 5.5	TTL	±4	20	50 pF	83	8	-40 to +125
74HC7731	Quad 64-bit shift register	2.0 to 6.0	CMOS	±5.2	15	50 pF	100	64	-40 to +125
74HCT7731	Quad 64-bit shift register; TTL-enabled	4.5 to 5.5	TTL	±4	20	50 pF	100	64	-40 to +125
74LV164	8-bit serial-in/parallel-out shift register	1.0 to 5.5	TTL	±12	12	50 pF	78	8	-40 to +125
74LV165	8-bit parallel or serial-in/serial-out shift register	1.0 to 5.5	TTL	±12	18	50 pF	78	8	-40 to +125
74LV4094	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	1.0 to 3.6	TTL	±6	14	50 pF	95	8	-40 to +125
74LV595	8-bit serial-in/parallel-out shift register with output storage register (3-state)	1.0 to 3.6	TTL	±8	15	50 pF	77	8	-40 to +125
74LVC594	8-bit serial-in/parallel-out shift register with output storage register	1.2 to 5.5	CMOS/ LVTTL	±24	3.1	50 pF	180	8	-40 to +125
74LVC595	8-bit serial-in/parallel-out shift register with output storage register (3-state)	1.2 to 5.5	CMOS/ LVTTL	±24	4	50 pF	180	8	-40 to +125
74VHC595	8-bit serial-in/parallel-out shift register with output storage register (3-state)	2.0 to 5.5	CMOS	±8	4	50 pF	170	8	-40 to +125
74VHCT595	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	3.8	50 pF	170	8	-40 to +125
HEF4014	8-bit shift register with synchronous parallel enable	4.5 to 15	CMOS	±2.4	40	50 pF	40	8	-40 to +85
HEF4015	dual 4-bit serial-in/parallel-out shift register	4.5 to 15	CMOS	±2.4	40	50 pF	44	4	-40 to +85
HEF4021	8-bit shift register with asynchronous parallel load	4.5 to 15	CMOS	±2.4	40	50 pF	40	8	-40 to +85
HEF4094	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	4.5 to 15	CMOS	±2.4	50	50 pF	28	8	-40 to +85
HEF4517	Dual 64-bit serial-in/parallel-out shift register	4.5 to 15	CMOS	±2.4	60	50 pF	16	64	-40 to +85
HEF4557	1-to-64-bit shift register with variable length	4.5 to 15	CMOS	±2.4	65	50 pF	20	64	-40 to +85
HEF4794	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 to 15	CMOS	-20	45	50 pF	28	8	-40 to +85
HEF4894	12-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 to 15	CMOS	20	45	50 pF	28	12	-40 to +85
NPIC6C4894	12-bit serial-in/parallel-out shift register with output storage register (3-state)	4.5 to 5.5	CMOS	100	90	30 pF	10	12	-40 to +125
NPIC6C595	8-bit serial-in/parallel-out shift register with output storage register (3-state)	4.5 to 5.5	CMOS	100	90	30 pF	10	8	-40 to +125
NPIC6C596	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 to 5.5	CMOS	100	90	30 pF	10	8	-40 to +125

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

TRANSCEIVERS

Features and benefits

- Bidirectional operation
- Mixed 3.3/5 V applications
- Widths from 4 to 32 bits
- Improve the current drive and signal levels
- Improve signal integrity in complex layouts
- Wide range of supply voltages
- Low propagation delay
- Registered options
- Optional TTL inputs, source-termination resistors, overvoltage-tolerant inputs, bus hold

Applications

- Parallel backplanes
- Telecommunications infrastructure
- Industrial control
- Test systems

Transceivers

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability	t_{pd} (ns)	Number of bits	f_{max} (MHz)	Output Load $C_{L\ (Typ)}$
74AHC245	Octal transceiver (3-state)	2.0 to 5.5	CMOS	±8	3.5	8	60	50 pF
74AHCT245	Octal transceiver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	5	8	60	50 pF
74ALVC16245	16-bit transceiver (3-state)	1.65 to 3.6	TTL	±24	1.9	16	150	50 pF
74ALVCH16245	16-bit transceiver with bus hold (3-state)	1.65 to 3.6	TTL	±24	1.9	16	150	50 pF
74ALVC245	Octal transceiver (3-state)	1.65 to 3.6	TTL	±24	2.3	8	130	50 pF
74ALVCH162245	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	1.65 to 3.6	TTL	±12	2.4	16	150	50 pF
74ALVCH162601	18-bit universal bus transceiver with bus hold and 30 Ω termination resistors; positive-edge trigger (3-state)	1.65 to 3.6	TTL	±12	3.1	18	150	50 pF
74ALVCH16500	18-bit universal bus transceiver with bus hold; negative edge trigger (3-state)	1.65 to 3.6	TTL	±24	2.9	18	150	50 pF
74ALVCH16501	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	1.65 to 3.6	TTL	±24	2.8	18	150	50 pF
74ALVCH16543	16-bit registered transceiver with bus hold (3-state)	1.65 to 3.6	TTL	±24	3.8	16	150	50 pF
74ALVCH16600	18-bit universal bus transceiver with bus hold; negative edge trigger (3-state)	1.65 to 3.6	TTL	±24	2.8	18	150	50 pF
74ALVCH16601	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	1.65 to 3.6	TTL	±24	2.8	18	150	50 pF
74ALVCH16646	16-bit registered transceiver with bus hold (3-state)	1.65 to 3.6	TTL	±24	2.6	16	150	50 pF
74ALVCH16952	16-bit registered transceiver with bus hold (3-state)	1.65 to 3.6	TTL	±24	3.2	16	150	50 pF
74ALVT162245	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	2.3 to 3.6	TTL	±12	2.3	16	75	50 pF
74ALVT16245	16-bit transceiver with bus hold (3-state)	2.3 to 3.6	TTL	-32 / +64	1.5	16	200	50 pF
74ALVT16501	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	2.3 to 3.6	TTL	-32 / +64	1.8	18	150	50 pF
74ALVT16543	16-bit registered transceiver with bus hold (3-state)	2.3 to 3.6	TTL	-32 / +64	1.8	16	200	50 pF
74ALVT16601	18-bit universal bus transceiver with bus hold; positive edge trigger (3-state)	2.3 to 3.6	TTL	-32 / +64	1.9	18	200	50 pF
74ALVT16652	16-bit registered transceiver with bus hold (3-state)	2.3 to 3.6	TTL	-32 / +64	2.4	16	150	50 pF

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Transceivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability	t_{pd} (ns)	Number of bits	f_{max} (MHz)	Output Load $C_{L\ (Typ)}$
74AVC16245	16-bit transceiver (3-state)	1.2 to 3.6	CMOS	±12	2	16	200	30 pF
74AVCH16245	16-bit transceiver with bus hold (3-state)	1.2 to 3.6	CMOS	±12	2	16	200	30 pF
74HC245	Octal transceiver (3-state)	2.0 to 6.0	CMOS	±7.8	7	8	36	50 pF
74HCT245	Octal transceiver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	10	8	36	50 pF
74HC640	Octal transceiver; inverting (3-state)	2.0 to 6.0	CMOS	±7.8	9	8	36	50 pF
74HCT640	Octal transceiver; inverting; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	9	8	36	50 pF
74HC652	Octal registered transceiver (3-state)	2.0 to 6.0	CMOS	±7.8	13	8	36	50 pF
74HCT652	Octal registered transceiver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±6	13	8	36	50 pF
74LV245	Octal transceiver (3-state)	1.0 to 5.5	TTL	±16	7	8	30	50 pF
74LVC162245	16-bit transceiver with 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	3.3	16	175	50 pF
74LVCH162245	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	3.3	16	175	50 pF
74LVC16245	16-bit transceiver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3	16	175	50 pF
74LVCH16245	16-bit transceiver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3	16	175	50 pF
74LVC245	Octal transceiver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	2.9	8	175	50 pF
74LVCH245	Octal transceiver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	2.9	8	175	50 pF
74LVC2245	Octal transceiver with 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	3.3	8	175	50 pF
74LVC2952	Octal registered transceiver with 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	4.3	8	175	50 pF
74LVC32245	32-bit transceiver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	2.2	32	175	50 pF
74LVC543	Octal registered transceiver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3.3	8	175	50 pF
74LVC544	Octal registered transceiver; inverting (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	4	8	175	50 pF
74LVC623	Octal transceiver with dual enable (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3.3	8	175	50 pF
74LVC646	Octal registered transceiver (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3.9	8	175	50 pF
74LVCH322245	32-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	1.2 to 3.6	CMOS/ LVTTL	±12	3.3	32	175	50 pF
74LVCH32245	32-bit transceiver with bus hold (3-state)	1.2 to 3.6	CMOS/ LVTTL	±24	3	32	175	50 pF
74LVT16245	16-bit transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	16	150	50 pF
74LVTH16245	16-bit transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	16	150	50 pF
74LVT2245	Octal transceiver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	3.2	8	150	50 pF

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Transceivers (cont.)

Type number	Description	V_{CC} (V)	Logic switching levels	Output drive capability	t_{pd} (ns)	Number of bits	f_{max} (MHz)	Output Load $C_{L\ (Typ)}$
74LVTH2245	Octal transceiver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	3.2	8	150	50 pF
74LVT162245	16-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	2.5	16	150	50 pF
74LVT16500	18-bit universal bus transceiver with bus hold; negative-edge trigger (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	18	150	50 pF
74LVT16501	18-bit universal bus transceiver with bus hold; positive-edge trigger (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	18	150	50 pF
74LVT16543	16-bit registered transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	2.2	16	150	50 pF
74LVT16646	16-bit registered transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	16	150	50 pF
74LVT16652	16-bit registered transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	16	150	50 pF
74LVT245	Octal transceiver (3-state)	2.7 to 3.6	TTL	-32 / +64	2.4	8	150	50 pF
74LVT2952	Octal registered transceiver with 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	-32 / +64	3.8	8	150	50 pF
74LVT543	Octal registered transceiver (3-state)	2.7 to 3.6	TTL	-32 / +64	3	8	150	50 pF
74LVT543	Octal registered transceiver (3-state)	2.7 to 3.6	TTL	-32 / +64	3	8	150	50 pF
74LVT640	Octal transceiver with bus hold; inverting (3-state)	2.7 to 3.6	TTL	-32 / +64	2.4	8	150	50 pF
74LVT646	Octal registered transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	3.8	8	150	50 pF
74LVT652	Octal registered transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	3.7	8	150	50 pF
74LVTH322245	32-bit transceiver with bus hold and 30 Ω termination resistors (3-state)	2.7 to 3.6	TTL	±12	2.5	32	150	50 pF
74LVTH32245	32-bit transceiver with bus hold (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	32	150	50 pF
74LVTN16245	16-bit transceiver (3-state)	2.7 to 3.6	TTL	-32 / +64	1.9	16	150	50 pF
74VHC245	Octal transceiver (3-state)	2.0 to 5.5	CMOS	±8	3.5	8	60	50 pF
74VHCT245	Octal transceiver; TTL-enabled (3-state)	4.5 to 5.5	TTL	±8	5	8	60	50 pF

Note: Selected package types only. Complete package listings are in the previous section and online at www.nxp.com/logic.

Q100 Standard Logic functions & packages

Standard logic functions include options suitable for use at supply voltage between 1.0 V and 15 V. They provide a wide range of functions such as analog switches, buffers/inverters, bus switches, counters, decoders/de-multiplexers, multiplexers, flip-flops, gates, latches, level shifters, multivibrators, Schmitt triggers, shift registers and transceivers. Q100 Standard logic is available in leaded SO and TSSOP packages as well as the innovative leadless DQFN package. NXP's DQFN packages include side-wettable flanks, making them suitable for automated optical inspection. *The package suffixes used in the tables are for all logic families with the exception of HEF4000B. The suffixes for HEF4000B can be found under Standard Logic Packages.*

Analog switches

Type number	Description	Features					Package (suffix)						
		Configuration	V_{CC} (V)	R_{ON} (Ω)	R_{ON} (FLAT) (Ω)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT403-1 (PW)	SOT763-1 (BQ)	SOT137-1 (D)
74HC4051-Q100	Single-pole, octal-throw analog switch	SP8T-Z	2.0 - 10.0	200	20	-40~125				•	•	•	
74HCT4051-Q100	Single-pole, octal-throw analog switch; TTL-enabled	SP8T-Z	4.5 - 5.5	225	20	-40~125				•	•	•	
74HC4052-Q100	Dual single-pole, quad-throw analog switch	SP4T-Z	2.0 - 10.0	200	20	-40~125				•	•	•	
74HCT4052-Q100	Dual single-pole, quad-throw analog switch; TTL-enabled	SP4T-Z	4.5 - 5.5	200	20	-40~125				•	•	•	
74HC4053-Q100	Triple single-pole, double-throw analog switch	SP8T-Z	2.0 - 10.0	200	20	-40~125				•	•	•	
74HCT4053-Q100	Triple single-pole, double-throw analog switch; TTL-enabled	SP8T-Z	4.5 - 5.5	200	20	-40~125				•	•	•	
74HC4066-Q100	Quad single-pole, single-throw analog switch	SPST-NO	2.0 - 10.0	105	23	-40~125	•	•	•				
74HCT4066-Q100	Quad single-pole, single-throw analog switch; TTL-enabled	SPST-NO	4.5 - 5.5	118	23	-40~125	•	•	•				
74HC4851-Q100	Single-pole, octal-throw analog switch	SP8T-Z	2.0 - 10.0	220	-	-40~125				•	•	•	
74HCT4851-Q100	Single-pole, octal-throw analog switch; TTL-enabled	SP8T-Z	4.5 - 5.5	240	-	-40~125				•	•	•	
74HC4852-Q100	Dual single-pole, quad-throw analog switch	SP4T-Z	2.0 - 10.0	220	-	-40~125				•	•	•	
74HCT4852-Q100	Dual single-pole, quad-throw analog switch; TTL-enabled	SP4T-Z	4.5 - 5.5	240	-	-40~125				•	•	•	
74LV4052-Q100	Dual single-pole, quad-throw analog switch	SP4T-Z	1.0 - 6.0	125	15	-40~125				•	•		
74LV4053-Q100	Triple single-pole, double-throw analog switch	SPDT-Z	1.0 - 6.0	150	30	-40~125				•	•	•	
74LVC4066-Q100	Quad single-pole, single-throw analog switch	SPST-NO	1.65 - 5.5	15	1.5	-40~125	•	•	•				
HEF4051B-Q100	Single-pole, octal-throw analog switch	SP8T-Z	4.5 - 15.5	175	30	-40~85				•	•		
HEF4052B-Q100	Dual single-pole, quad-throw analog switch	SP4T-Z	4.5 - 15.5	175	30	-40~85				•	•		
HEF4053B-Q100	Triple single-pole, double-throw analog switch	SPDT-Z	4.5 - 15.5	175	30	-40~85				•	•		
HEF4066B-Q100	Quad single-pole, single-throw analog switch	SPST-NO	4.5 - 15.5	175	20	-40~85	•						
HEF4067B-Q100	Single-pole, 16-throw analog switch	SP16T-Z	4.5 - 15.5	175	20	-40~85							•

Buffers/inverters

Type number	Description	Features				Package (suffix)										
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT403-1 (PW)	SOT163-1 (D)	SOT339-1 (DB)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)
74AHC04-Q100	Hex inverter	2.0 - 5.5	± 8	3	-40~125	•		•	•							
74AHCT04-Q100	Hex inverter; TTL-enabled	4.5 - 5.5	± 8	3	-40~125	•		•	•							
74AHC125-Q100	Quad buffer/line driver (3-state)	2.0 - 5.5	± 8	3	-40~125	•		•	•							
74AHCT125-Q100	Quad buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3	-40~125	•		•	•							
74AHC126-Q100	Quad buffer/line driver (3-state)	2.0 - 5.5	± 8	3.3	-40~125	•		•	•							
74AHCT126-Q100	Quad buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3	-40~125	•		•	•							
74AHC240-Q100	Octal inverter/line driver (3-state)	2.0 - 5.5	± 8	2.8	-40~125							•		•	•	
74AHCT240-Q100	Octal inverter/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3	-40~125							•		•	•	
74AHC244-Q100	Octal buffer/line driver (3-state)	2.0 - 5.5	± 8	3.5	-40~125							•		•	•	
74AHCT244-Q100	Octal buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.5	-40~125							•		•	•	
74AHC541-Q100	Octal buffer/line driver (3-state)	2.0 - 5.5	± 8	3.5	-40~125							•		•	•	
74AHCT541-Q100	Octal buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.5	-40~125							•		•	•	
74AHCU04-Q100	Hex inverter; unbuffered	2.0 - 5.5	± 8	2.4	-40~125	•		•	•							
74ALVC125-Q100	Quad buffer/line driver (3-state)	1.65 - 3.6	± 24	1.8	-40~85	•		•	•							
74ALVC541-Q100	Octal buffer/line driver (3-state)	1.65 - 3.6	± 24	2.3	-40~85							•		•	•	
74HC05-Q100	Hex inverter; open-drain	2.0 - 6.0	5.2	11	-40~125	•		•	•							
74HC04-Q100	Hex inverter	2.0 - 6.0	± 5.2	7	-40~125	•	•	•	•							
74HCT04-Q100	Hex inverter; TTL-enabled	4.5 - 5.5	± 4.0	8	-40~125	•		•	•							
74HC125-Q100	Quad buffer/line driver (3-state)	2.0 - 6.0	± 7.8	9	-40~125	•		•								
74HCT125-Q100	Quad buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	12	-40~125	•		•								
74HC126-Q100	Quad buffer/line driver (3-state)	2.0 - 6.0	± 7.8	9	-40~125	•		•								
74HCT126-Q100	Quad buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	11	-40~125	•		•								
74HC240-Q100	Octal inverter/line driver (3-state)	2.0 - 6.0	± 7.8	9	-40~125							•		•	•	
74HCT240-Q100	Octal inverter/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	9	-40~125							•		•	•	
74HC244-Q100	Octal buffer/line driver (3-state)	2.0 - 6.0	± 7.8	9	-40~125							•		•	•	
74HCT244-Q100	Octal buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	11	-40~125							•		•	•	
74HC365-Q100	Hex buffer/line driver (3-state)	2.0 - 6.0	± 7.8	9	-40~125					•	•					
74HCT365-Q100	Hex buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	11	-40~125					•	•					
74HC366-Q100	Hex inverter/line driver (3-state)	2.0 - 6.0	± 7.8	10	-40~125					•	•					
74HCT366-Q100	Hex inverter/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	11	-40~125					•	•					

Buffers/inverters (cont.)

Type number	Description	Features				Package (suffix)										
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT403-1 (PW)	SOT163-1 (D)	SOT339-1 (DB)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)
74HC540-Q100	Octal inverter/line driver (3-state)	2.0 - 6.0	± 7.8	9	-40~125							•				
74HCT540-Q100	Octal inverter/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	11	-40~125							•				
74HC541-Q100	Octal buffer/line driver (3-state)	2.0 - 6.0	± 7.8	10	-40~125							•		•		
74HCT541-Q100	Octal buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 6	12	-40~125							•		•		
74HCU04-Q100	Hex inverter; unbuffered	2.0 - 6.0	± 5.2	5	-40~125	•		•	•							
74LV244-Q100	Octal buffer/line driver (3-state)	1.0 - 5.5	± 16	8	-40~125							•		•		
74LVC04A-Q100	Hex inverter	1.65 - 5.5	± 24	2	-40~125	•		•	•							
74LVC06A-Q100	Hex inverter; open-drain	1.65 - 5.5	32	2.2	-40~125	•		•	•							
74LVC07A-Q100	Hex buffer; open-drain	1.65 - 5.5	32	2.2	-40~125	•		•	•							
74LVC125A-Q100	Quad buffer/line driver (3-state)	1.2 - 3.6	± 24	2.4	-40~125	•		•	•							
74LVC126A-Q100	Quad buffer/line driver (3-state)	1.2 - 3.6	± 24	2.4	-40~125	•		•	•							
74LVC541A-Q100	Octal buffer/line driver (3-state)	1.2 - 3.6	± 24	3.3	-40~125							•		•	•	
74LVC16240A-Q100	16-bit inverter/line driver (3-state)	1.2 - 3.6	± 24	2.7	-40~125											•
74LVC244A-Q100	Octal buffer/line driver (3-state)	1.2 - 3.6	± 24	2.8	-40~125							•	•	•	•	
74LVCH244A-Q100	Octal buffer/line driver with bus hold (3-state)	1.2 - 3.6	± 24	2.8	-40~125							•		•	•	
74LVC16244A-Q100	16-bit buffer/line driver (3-state)	1.2 - 3.6	± 24	3	-40~125											•
74LVCH16244A-Q100	16-bit buffer/line driver with bus hold (3-state)	1.2 - 3.6	± 24	3	-40~125											•
74LVT04-Q100	Hex inverter	2.7 - 3.6	-20 / +32	2.6	-40~85	•	•	•								
74LVT244A-Q100	Octal buffer/line driver with bus hold (3-state)	2.7 - 3.6	-32 / +64	2.6	-40~85							•		•		
74LVTH244A-Q100	Octal buffer/line driver with bus hold (3-state)	2.7 - 3.6	-32 / +64	2.6	-40~85							•		•		
74VHC126-Q100	Quad buffer/line driver (3-state)	2.0 - 5.5	± 8	3.3	-40~125	•		•	•							
74VHCT126-Q100	Quad buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3	-40~125	•		•	•							
74VHC541-Q100	Octal buffer/line driver (3-state)	2.0 - 5.5	± 8	3.5	-40~125							•		•	•	
74VHCT541-Q100	Octal buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.5	-40~125							•		•	•	
HEF4049B-Q100	Hex inverter/line driver	3.0 - 15.0	-3 / +20	20	-40~85					•						
HEF4050B-Q100	Hex buffer/line driver	3.0 - 15.0	-3 / +20	40	-40~85					•						
HEF4069UB-Q100	Hex inverter; unbuffered	3.0 - 15.0	± 3.4	15	-40~85	•		•								

Bus switches

Type number	Description	Features				Package (suffix)								
		V_{CC} (V)	V_{PASS} (V)	R_{ON} (Ω)	T_{amb} (°C)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT403-1 (PW)	SOT519-1 (DS)	SOT763-1 (BQ)	SOT163-1 (D)	SOT360-1 (PW)	SOT764-1 (BQ)
74CBTLV3126-Q100	Quad bus switch	2.3 - 3.6	3.3	7	-40~125	•	•							
74CBTLV3253-Q100	Dual 4:1 mux/demux	2.3 - 3.6	3.3	7	-40~125			•	•		•			
74CBTLV3257-Q100	Quad 2:1 mux/demux	2.3 - 3.6	3.3	7	-40~125			•	•	•	•			
CBT3245A-Q100	Octal bus switch	4.5 - 5.5	3.9	7	-40~85							•	•	•

Counters/frequency dividers

Type number	Description	Features				Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)
74HC4024-Q100	7-stage binary ripple counter	2.0 - 6.0	± 5.2	14	-40~125	•	•					
74HC163-Q100	Presettable synchronous 4-bit binary counter; synchronous reset	2.0 - 6.0	± 5.2	17	-40~125				•		•	
74HCT163-Q100	Presettable synchronous 4-bit binary counter; synchronous reset; TTL-enabled	4.5 - 5.5	± 4.0	20	-40~125				•		•	
74HC193-Q100	Presettable synchronous 4-bit binary up/down counter	2.0 - 6.0	± 5.2	20	-40~125				•	•	•	
74HCT193-Q100	Presettable synchronous 4-bit binary up/down counter; TTL-enabled	4.5 - 5.5	± 4.0	20	-40~125				•	•	•	
74HC393-Q100	Dual 4-bit binary ripple counter	2.0 - 6.0	± 5.2	12	-40~125	•	•	•				
74HCT393-Q100	Dual 4-bit binary ripple counter; TTL-enabled	4.5 - 5.5	± 4.0	20	-40~125	•	•	•				
74HC4017-Q100	Johnson decade counter with 10 decoded outputs	2.0 - 6.0	± 5.2	18	-40~125				•		•	•
74HCT4017-Q100	Johnson decade counter with 10 decoded outputs; TTL-enabled	4.5 - 5.5	± 4.0	21	-40~125				•			•
74HC4020-Q100	14-stage binary ripple counter	2.0 - 6.0	± 5.2	11	-40~125				•		•	•
74HCT4020-Q100	14-stage binary ripple counter; TTL-enabled	4.5 - 5.5	± 4.0	15	-40~125				•		•	•
74HC4040-Q100	12-stage binary ripple counter	2.0 - 6.0	± 5.2	14	-40~125				•	•	•	•
74HCT4040-Q100	12-stage binary ripple counter; TTL-enabled	4.5 - 5.5	± 4.0	16	-40~125				•	•	•	•
74HC4060-Q100	14-stage binary ripple counter with oscillator	2.0 - 6.0	± 5.2	31	-40~125					•	•	•
74HCT4060-Q100	14-stage binary ripple counter with oscillator; TTL-enabled	4.5 - 5.5	± 4.0	31	-40~125				•			•
74HC4520-Q100	Dual 4-bit synchronous binary counter	2.0 - 6.0	± 5.2	24	-40~125				•		•	
74HCT4520-Q100	Dual 4-bit synchronous binary counter; TTL-enabled	4.5 - 5.5	± 4.0	24	-40~125				•			
74LV393-Q100	Dual 4-bit binary ripple counter	1.0 - 3.6	± 6	12	-40~125	•	•					

Counters/frequency dividers (cont.)

Type number	Description	Features				Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)
HEF4017B-Q100	5-stage Johnson decade counter	4.5 - 15.5	± 2.4	40	-40~85				•			
HEF4020B-Q100	14-stage binary ripple counter	4.5 - 15.5	± 2.4	30	-40~85				•			
HEF4040B-Q100	12-stage binary ripple counter	4.5 - 15.5	± 2.4	35	-40~85				•			
HEF4060B-Q100	14-stage binary ripple counter with oscillator	4.5 - 15.5	± 2.4	50	-40~85				•			
HEF4541B-Q100	programmable timer	4.5 - 15.5	- 4/ + 2.7	38	-40~85	•						

Digital decoders/demultiplexers

Type number	Description	Features				Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)
74AHC138-Q100	3-to-8 line decoder/demultiplexer; inverting	2.0 - 5.5	± 8	4.4	-40~125	•		•	•
74AHCT138-Q100	3-to-8 line decoder/demultiplexer; inverting; TTL-enabled	4.5 - 5.5	± 8	4.4	-40~125	•		•	•
74AHC139-Q100	Dual 2-to-4 line decoder/demultiplexer	2.0 - 5.5	± 8	3.9	-40~125	•		•	
74AHCT139-Q100	Dual 2-to-4 line decoder/demultiplexer; TTL-enabled	4.5 - 5.5	± 8	3.6	-40~125	•		•	
74HC237-Q100	3-to-8 decoder/demultiplexer with address latches	2.0 - 6.0	± 5.2	18	-40~125	•			
74HC138-Q100	3-to-8 line decoder/demultiplexer; inverting	2.0 - 6.0	± 5.2	12	-40~125	•		•	•
74HCT138-Q100	3-to-8 line decoder/demultiplexer; inverting; TTL-enabled	4.5 - 5.5	± 4	19	-40~125	•		•	•
74HC139-Q100	Dual 2-to-4 line decoder/demultiplexer	2.0 - 6.0	± 5.2	14	-40~125	•	•	•	
74HCT139-Q100	Dual 2-to-4 line decoder/demultiplexer; TTL-enabled	4.5 - 5.5	± 4	16	-40~125	•	•	•	
74HC238-Q100	3-to-8 decoder/demultiplexer	2.0 - 6.0	± 5.2	14	-40~125	•		•	•
74HCT238-Q100	3-to-8 decoder/demultiplexer; TTL-enabled	4.5 - 5.5	± 4	18	-40~125	•		•	•
74LVC138A-Q100	3-to-8 line decoder/demultiplexer; inverting	1.2 - 3.6	± 24	2.7	-40~125	•		•	•
HEF4555B-Q100	Dual 1-to-4 line decoder/demultiplexer	4.5 - 15	± 2.4	30	-40~85	•			

Digital multiplexers

Type number	Description	Features				Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)
74AHC157-Q100	Quad 2-input multiplexer	2.0 - 5.5	± 8	3.2	-40~125	•		•	•
74AHCT157-Q100	Quad 2-input multiplexer; TTL-enabled	4.5 - 5.5	± 8	3.2	-40~125	•		•	•
74AHC257-Q100	Quad 2-input multiplexer (3-State)	2.0 - 5.5	± 8	2.9	-40~125	•		•	
74AHCT257-Q100	Quad 2-input multiplexer; TTL-enabled (3-State)	4.5 - 5.5	± 8	3.7	-40~125	•		•	
74HC151-Q100	8-input multiplexer	2.0 - 6.0	± 5.2	17	-40~125	•		•	
74HCT151-Q100	8-input multiplexer; TTL-enabled	4.5 - 5.5	± 4	19	-40~125	•		•	
74HC153-Q100	Dual 4-input multiplexer	2.0 - 6.0	± 5.2	17	-40~125	•		•	
74HCT153-Q100	Dual 4-input multiplexer; TTL-enabled	4.5 - 5.5	± 4	19	-40~125	•		•	
74HC157-Q100	Quad 2-input multiplexer	2.0 - 6.0	± 5.2	11	-40~125	•		•	•
74HCT157-Q100	Quad 2-input multiplexer; TTL-enabled	4.5 - 5.5	± 4	13	-40~125	•		•	•
74HC251-Q100	8-input multiplexer (3-State)	2.0 - 6.0	± 5.2	18	-40~125	•		•	
74HCT251-Q100	8-input multiplexer; TTL-enabled (3-State)	4.5 - 5.5	± 4	22	-40~125	•		•	
74HC253-Q100	Dual 4-input multiplexer (3-State)	2.0 - 6.0	± 7.8	17	-40~125	•			
74HCT253-Q100	Dual 4-input multiplexer; TTL-enabled (3-State)	4.5 - 5.5	± 6	17	-40~125	•			
74LVC157A-Q100	Quad 2-input multiplexer	1.2 - 3.6	± 24	2.5	-40~125	•	•	•	•

Flip-flops

Type number	Description	Features				Package (suffix)										
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT162-1 (D)	SOT403-1 (PW)	SOT163-1 (D)	SOT339-1 (DB)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)
74AHC74-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger	2.0 - 5.5	± 8	3.7	-40~125	•		•	•								
74AHCT74-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 8	3.3	-40~125	•		•	•								
74AHC273-Q100	Octal D-type flip-flop with reset; positive-edge trigger	2.0 - 5.5	± 8	4.2	-40~125								•		•	•	
74AHCT273-Q100	Octal D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 8	4	-40~125								•		•	•	
74AHC374-Q100	Octal D-type flip-flop; positive-edge trigger	2.0 - 5.5	± 8	4.4	-40~125								•		•		
74AHCT374-Q100	Octal D-type flip-flop; positive-edge trigger (3-state); TTL-enabled (3-state)	4.5 - 5.5	± 8	4.3	-40~125								•		•		
74AHC377-Q100	Octal D-type flip-flop with data enable; positive-edge trigger	2.0 - 5.5	± 8	3.9	-40~125										•		

Flip-flops (cont.)

Type number	Description	Features				Package (suffix)											
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT162-1 (D)	SOT403-1 (PW)	SOT163-1 (D)	SOT339-1 (DB)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)
74AHCT377-Q100	Octal D-type flip-flop with data enable; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 8	4	-40~125								•		•		
74AVC16374-Q100	16-bit D-type flip-flop; positive-edge trigger (3-state)	1.2 - 3.6	± 12	1.5	-40~85												•
74HC74-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger	2.0 - 6.0	± 5.2	14	-40~125	•		•	•								
74HCT74-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 4	15	-40~125	•		•	•								
74HC107-Q100	Dual J-K flip-flop with reset; negative-edge trigger	2.0 - 6.0	± 5.2	16	-40~125	•		•									
74HCT107-Q100	Dual J-K flip-flop with reset; negative-edge trigger; TTL-enabled	4.5 - 5.5	± 4	16	-40~125	•											
74HC174-Q100	Hex D-type flip-flop with reset; positive-edge trigger	2.0 - 6.0	± 5.2	17	-40~125					•		•					
74HCT174-Q100	Hex D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 4	18	-40~125					•		•					
74HC175-Q100	Quad D-type flip-flop with reset; positive-edge trigger	2.0 - 6.0	± 5.2	17	-40~125					•		•					
74HCT175-Q100	Quad D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 4	16	-40~125					•		•					
74HC273-Q100	Octal D-type flip-flop with reset; positive-edge trigger	2.0 - 6.0	± 5.2	15	-40~125								•		•	•	
74HCT273-Q100	Octal D-type flip-flop with reset; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 4	15	-40~125								•		•	•	
74HC377-Q100	Octal D-type flip-flop with data enable; positive-edge trigger	2.0 - 6.0	± 7.8	13	-40~125								•	•	•		
74HCT377-Q100	Octal D-type flip-flop with data enable; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 6	14	-40~125								•	•	•		
74HC574-Q100	Octal D-type flip-flop; positive-edge trigger (3-state)	2.0 - 6.0	± 7.8	14	-40~125								•		•		
74HCT574-Q100	Octal D-type flip-flop; positive-edge trigger; TTL-enabled (3-state)	4.5 - 5.5	± 6	15	-40~125								•		•		
74LV74-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger	1.0 - 5.5	± 12	11	-40~125	•		•									

Flip-flops (cont.)

Type number	Description	Features				Package (suffix)										
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT162-1 (D)	SOT403-1 (PW)	SOT163-1 (D)	SOT339-1 (DB)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)
74LVC74A-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger	1.2 - 3.6	± 24	2.5	-40~125	•		•	•								
74LVC273-Q100	Octal D-type flip-flop with reset; positive-edge trigger	1.2 - 3.6	± 24	6	-40~125								•		•	•	
74LVC374A-Q100	Octal D-type flip-flop; positive-edge trigger (3-state)	1.2 - 3.6	± 24	2.7	-40~125								•		•	•	
74LVC573A-Q100	Octal D-type transparent latch (3-state)	1.2 - 3.6	± 24	3.4	-40~125								•		•	•	
74LVC16374A-Q100	16-bit D-type flip-flop; positive-edge trigger (3-state)	1.2 - 3.6	± 24	3.8	-40~125												•
74LVCH16374A-Q100	16-bit D-type flip-flop with bus hold; positive-edge trigger (3-state)	1.2 - 3.6	± 24	3.8	-40~125												•
HEF4013B-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger	4.5 - 15.5	± 2.4	30	-40~85	•		•									
HEF4027B-Q100	Dual J-K flip-flop	4.5 - 15.5	± 2.4	30	-40~85					•							

Gates (cont.)

Type number	Description	Features				Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)
74AHC00-Q100	Quad 2-input NAND gate	2.0 - 5.5	± 8	3.2	-40~125	•		•	•
74AHCT00-Q100	Quad 2-input NAND gate; TTL-enabled	4.5 - 5.5	± 8	3.3	-40~125	•		•	•
74AHC02-Q100	Quad 2-input NOR gate	2.0 - 5.5	± 8	2.9	-40~125	•		•	•
74AHCT02-Q100	Quad 2-input NOR gate; TTL-enabled	4.5 - 5.5	± 8	3.8	-40~125	•		•	•
74AHC08-Q100	Quad 2-input AND gate	2.0 - 5.5	± 8	3.5	-40~125	•		•	•
74AHCT08-Q100	Quad 2-input AND gate; TTL-enabled	4.5 - 5.5	± 8	5	-40~125	•		•	•
74AHC30-Q100	8-input NAND gate	2.0 - 5.5	± 8	3.6	-40~125	•		•	•
74AHCT30-Q100	8-input NAND gate; TTL-enabled	4.5 - 5.5	± 8	3.3	-40~125	•		•	•
74AHC32-Q100	Quad 2-input OR gate	2.0 - 5.5	± 8	3.5	-40~125	•		•	•
74AHCT32-Q100	Quad 2-input OR gate; TTL-enabled	4.5 - 5.5	± 8	5	-40~125	•		•	•
74AHC86-Q100	Quad 2-input EXCLUSIVE-OR gate	2.0 - 5.5	± 8	3.4	-40~125	•		•	•
74AHCT86-Q100	Quad 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 - 5.5	± 8	3.4	-40~125	•		•	•

Gates (cont.)

Type number	Description	Features				Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)
74ALVC00-Q100	Quad 2-input NAND gate	1.65-3.6	± 24	2.1	-40~85	•		•	•
74ALVC32-Q100	Quad 2-input OR gate	1.65 - 3.6	± 24	2	-40~125	•		•	•
74HC00-Q100	Quad 2-input NAND gate	2.0 - 6.0	± 5.2	7	-40~125	•		•	•
74HCT00-Q100	Quad 2-input NAND gate; TTL-enabled	4.5 - 5.5	± 4	10	-40~125	•		•	•
74HC02-Q100	Quad 2-input NOR gate	2.0 - 6.0	± 5.2	7	-40~125	•		•	•
74HCT02-Q100	Quad 2-input NOR gate; TTL-enabled	4.5 - 5.5	± 4	9	-40~125	•		•	•
74HC03-Q100	Quad 2-input NAND gate; open-drain	2.0 - 6.0	5.2	8	-40~125	•	•	•	
74HCT03-Q100	Quad 2-input NAND gate; open-drain; TTL-enabled	4.5 - 5.5	± 4	10	-40~125	•		•	
74HC08-Q100	Quad 2-input AND gate	2.0 - 6.0	± 5.2	7	-40~125	•		•	•
74HCT08-Q100	Quad 2-input AND gate; TTL-enabled	4.5 - 5.5	± 4	11	-40~125	•		•	•
74HC10-Q100	Triple 3-input NAND gate	2.0 - 6.0	± 5.2	9	-40~125	•		•	
74HCT10-Q100	Triple 3-input NAND gate; TTL-enabled	4.5 - 5.5	± 4	11	-40~125	•		•	
74HC11-Q100	Triple 3-input AND gate	2.0 - 6.0	± 5.2	10	-40~125	•		•	
74HCT11-Q100	Triple 3-input AND gate; TTL-enabled	4.5 - 5.5	± 4	11	-40~125	•		•	
74HC20-Q100	Dual 4-input NAND gate	2.0 - 6.0	± 5.2	8	-40~125	•		•	
74HCT20-Q100	Dual 4-input NAND gate; TTL-enabled	4.5 - 5.5	± 4	13	-40~125	•			•
74HC27-Q100	Triple 3-input NOR gate	2.0 - 6.0	± 5.2	8	-40~125	•		•	•
74HCT27-Q100	Triple 3-input NOR gate; TTL-enabled	4.5 - 5.5	± 4	10	-40~125	•		•	•
74HC30-Q100	8-input NAND gate	2.0 - 6.0	± 5.2	12	-40~125	•		•	
74HCT30-Q100	8-input NAND gate; TTL-enabled	4.5 - 5.5	± 4	12	-40~125	•		•	
74HC32-Q100	Quad 2-input OR gate	2.0 - 6.0	± 5.2	6	-40~125	•		•	•
74HCT32-Q100	Quad 2-input OR gate; TTL-enabled	4.5 - 5.5	± 4.0	9	-40~125	•		•	•
74HC86-Q100	Quad 2-input EXCLUSIVE-OR gate	2.0 - 6.0	± 5.2	11	-40~125	•		•	
74HCT86-Q100	Quad 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 - 5.5	± 4	14	-40~125	•		•	
74HC4002-Q100	Dual 4-input NOR gate	2.0 - 6.0	± 5.2	9	-40~125	•		•	
74HC4075-Q100	Triple 3-input OR gate	2.0 - 6.0	± 5.2	8	-40~125	•		•	
74HCT4075-Q100	Triple 3-input OR gate; TTL-enabled	4.5 - 5.5	± 4	10	-40~125	•		•	
74LV08-Q100	Quad 2-input AND gate	1.0 - 5.5	± 12	7	-40~125	•		•	
74LVC00A-Q100	Quad 2-input NAND gate	1.2 - 3.6	± 24	2.1	-40~125	•		•	•
74LVC02A-Q100	Quad 2-input NOR gate	1.2 - 3.6	± 24	2.1	-40~125	•		•	•
74LVC08A-Q100	Quad 2-input AND gate	1.2 - 3.6	± 24	2.1	-40~125	•		•	•
74LVC32A-Q100	Quad 2-input OR gate	1.2 - 3.6	± 24	2.1	-40~125	•	•	•	•
74VHC02-Q100	Quad 2-input NOR gate	2.0 - 5.5	± 8	2.9	-40~125	•		•	•
74VHCT02-Q100	Quad 2-input NOR gate; TTL-enabled	4.5 - 5.5	± 8	3.8	-40~125	•		•	•

Gates (cont.)

Type number	Description	Features				Package (suffix)			
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT337-1 (DB)	SOT402-1 (PW)	SOT762-1 (BQ)
74VHC08-Q100	Quad 2-input AND gate	2.0 - 5.5	± 8	3.5	-40~125	•		•	
74VHCT08-Q100	Quad 2-input AND gate; TTL-enabled	4.5 - 5.5	± 8	5	-40~125	•		•	•
74VHC32-Q100	Quad 2-input OR gate	2.0 - 5.5	± 8	3.5	-40~125	•		•	
74VHCT32-Q100	Quad 2-input OR gate; TTL-enabled	4.5 - 5.5	± 8	5	-40~125	•		•	•
HEF4001B-Q100	Quad 2-input NOR gate	4.5 - 15.5	± 2.4	20	-40~85	•			
HEF4011B-Q100	Quad 2-input NAND gate	4.5 - 15.5	± 2.4	20	-40~85	•			
HEF4030B-Q100	Quad 2-input EXCLUSIVE-OR gate	4.5 - 15.5	± 2.4	30	-40~85	•			
HEF4070B-Q100	Quad 2-input EXCLUSIVE-OR gate	4.5 - 15.5	± 2.4	30	-40~85	•			
HEF4081B-Q100	Quad 2-input AND gate	4.5 - 15.5	± 2.4	20	-40~85	•			

Latches/registered drivers

Type number	Description	Features				Package (suffix)							
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT109-1 (D)	SOT403-1 (PW)	SOT763-1 (BQ)	SOT163-1 (D)	SOT339-1 (DB)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)
74AHC573-Q100	Octal D-type transparent latch (3-state)	2.0 - 5.5	± 8	4.2	-40~125				•		•	•	
74AHCT573-Q100	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.9	-40~125				•		•	•	
74HC4060-Q100	14-stage binary ripple counter with oscillator	2.0 - 6.0	± 5.2	31	-40~125	•							
74HC259-Q100	8 bit addressable latch	2.0 - 6.0	± 5.2	18	-40~125	•	•	•					
74HCT259-Q100	8-Bit addressable latch; TTL-enabled	4.5 - 5.5	± 4	20	-40~125	•	•	•					
74HC373-Q100	Octal D-type transparent latch (3-state)	2.0 - 6.0	± 7.8	12	-40~125				•		•	•	
74HCT373-Q100	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 - 5.5	± 6	14	-40~125				•		•	•	
74HC573-Q100	Octal D-type transparent latch (3-state)	2.0 - 6.0	± 7.8	14	-40~125				•	•	•	•	
74HCT573-Q100	Octal D-type transparent latch; TTL-enabled (3-state)	4.5 - 5.5	± 6	17	-40~125				•		•	•	
74LVC373A-Q100	Octal D-type transparent latch (3-state)	1.2 - 3.6	± 24	3	-40~125				•	•	•	•	
74LVC16373A-Q100	16-bit D-type transparent latch (3-state)	1.2 - 3.6	± 24	2.4	-40~125								•
74LVCH16373A-Q100	16-bit D-type transparent latch with bushold (3-state)	1.2 - 3.6	± 24	2.4	-40~125								•
HEF4043B-Q100	Quad R/S latch with set and reset (3-state)	4.5 - 15	± 2.4	25	-40~85	•							

Level shifters/translators

Type number	Description	Features				Package (suffix)							
		V_{CC}(A) (V)	V_{CC}(B) (V)	I_O (mA)	T_{amb} (°C)	SOT109-1 (D)	SOT403-1 (PW)	SOT763-1 (BQ)	SOT137-1 (D)	SOT355-1 (PW)	SOT815-1 (BQ)	SOT362-1 (DGG)	SOT480-1 (DGV)
74ALVC164245-Q100	16-bit dual-supply voltage level translating transceiver (3-state)	1.5 - 3.6	1.5 - 5.5	± 24	-40~125							•	
74AVC4T245-Q100	4-bit dual-supply voltage level translating transceiver (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125	•	•	•					
74AVC8T245-Q100	8-bit dual-supply voltage level translating transceiver (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125					•	•		
74AVC16T245-Q100	16-bit dual-supply voltage level translating transceiver (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125								•
74AVCH4T245-Q100	4-bit dual-supply voltage translating transceiver with bus hold (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125	•	•	•					
74HC4050-Q100	Hex buffer with 15V tolerant inputs	2.0 - 6.0	n.a	± 5.2	-40~125	•	•						
74LVC4245A-Q100	8-bit dual-supply voltage translating transceiver (3-state)	1.5 - 5.5	1.5 - 3.6	± 24	-40~125				•	•	•		
74LVC8T245-Q100	8-bit dual-supply voltage translating transceiver (3-state)	1.2 - 5.5	1.2 - 5.5	± 24	-40~125					•	•		
74LVCH8T245-Q100	8-bit dual-supply voltage translating transceiver with bus hold (3-state)	1.2 - 5.5	1.2 - 5.5	± 24	-40~125					•	•		
HEF4104B-Q100	Quad low-to-high voltage translator (3-state)	3.0 - 15.0	3.0 - 15.0	± 2.4	-40~85	•							

Multivibrators

Type number	Description	Features				Package (suffix)		
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT109-1 (D)	SOT403-1 (PW)	SOT763-1 (BQ)
74AHC123A-Q100	Dual retriggerable monostable multivibrator with reset	2.0 - 5.5	± 8	5.1	-40~125	•	•	•
74AHCT123A-Q100	Dual retriggerable monostable multivibrator with reset; TTL-enabled	4.5 - 5.5	± 8	5	-40~125	•	•	•
74HC123-Q100	Dual retriggerable monostable multivibrator with reset	2.0 - 6.0	± 7.8	9	-40~125	•	•	•
74HCT123-Q100	Dual retriggerable monostable multivibrator with reset; TTL-enabled	4.5 - 5.5	± 4	26	-40~125	•	•	
74HC4538-Q100	Dual retriggerable precision monostable multivibrator	2.0 - 6.0	± 5.2	27	-40~125	•	•	
74HCT4538-Q100	Dual retriggerable precision monostable multivibrator; TTL-enabled	4.5 - 5.5	± 4	30	-40~125	•	•	
HEF4538B-Q100	Dual retriggerable precision monostable multivibrator	4.5 - 15.5	± 2.4	60	-40~85	•		

Schmitt triggers

Type number	Description	Features				Package (suffix)				
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT163-1 (D)	SOT360-1 (PW)
74AHC14-Q100	Hex inverter Schmitt trigger	2.0 - 5.5	± 8	3.2	-40~125	•	•	•		
74AHCT14-Q100	Hex inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 8	4	-40~125	•	•	•		
74AHC132-Q100	Quad 2-input NAND gate Schmitt trigger	2.0 - 5.5	± 8	3.3	-40~125	•	•	•		
74AHCT132-Q100	Quad 2-input NAND gate Schmitt trigger; TTL-enabled	4.5 - 5.5	± 8	3.5	-40~125	•	•	•		
74HC7014-Q100	Hex buffer precision Schmitt trigger	2.0 - 6.0	± 5.2	27	-40~125	•				
74HC14-Q100	Hex inverter Schmitt trigger	2.0 - 6.0	± 5.2	12	-40~125	•	•	•		
74HCT14-Q100	Hex inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 4	17	-40~125	•	•	•		
74HC132-Q100	Quad 2-input NAND gate Schmitt trigger	2.0 - 6.0	± 5.2	11	-40~125	•	•			
74HCT132-Q100	Quad 2-input NAND gate Schmitt trigger; TTL-enabled	4.5 - 5.5	± 4	17	-40~125	•	•			
74HC7541-Q100	Octal buffer/line driver Schmitt trigger (3-State)	2.0 - 6.0	± 7.8	11	-40~125				•	•
74HCT7541-Q100	Octal buffer/line driver Schmitt trigger; TTL-enabled (3-State)	4.5 - 5.5	± 6	16	-40~125				•	•
74LV132-Q100	Quad 2-input NAND gate Schmitt trigger	1.0 - 5.5	± 12	10	-40~125	•	•	•		
74LVC14A-Q100	Hex inverter Schmitt trigger	1.2 - 3.6	± 24	3.2	-40~125	•	•	•		
74LVC132A-Q100	Quad 2-input NAND gate Schmitt trigger	1.2 - 3.6	± 24	3.4	-40~125	•	•	•		
HEF40106B-Q100	Hex inverter Schmitt trigger	4.5 - 15.5	± 2.4	30	-40~85	•	•			

Shift registers

Type number	Description	Features				Package (suffix)								
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)	SOT163-1 (D)	SOT360-1 (PW)
74AHC164-Q100	8-bit serial-in/parallel-out shift register	2.0 - 5.5	± 8	4.5	-40~125	•	•	•						
74AHCT164-Q100	8-bit serial-in/parallel-out shift register; TTL-enabled	4.5 - 5.5	± 8	3.4	-40~125	•	•	•						
74AHC594-Q100	8-bit serial-in/parallel-out shift register with output register	2.0 - 5.5	± 8	4.1	-40~125				•	•	•	•		
74AHCT594-Q100	8-bit serial-in/parallel-out shift register with output register; TTL-enabled	4.5 - 5.5	± 8	3.8	-40~125				•	•	•	•		
74AHC595-Q100	8-bit serial-in/parallel-out shift register with output register (3-state)	2.0 - 5.5	± 8	4	-40~125				•		•	•		
74AHCT595-Q100	8-bit serial-in/parallel-out shift register with output storage; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.8	-40~125				•		•	•		
74HC164-Q100	8-bit serial-in/parallel-out shift register	2.0 - 6.0	± 5.2	12	-40~125	•	•	•						

Shift registers (cont.)

Type number	Description	Features				Package (suffix)								
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)	SOT163-1 (D)	SOT360-1 (PW)
74HCT164-Q100	8-bit serial-in/parallel-out shift register; TTL-enabled	4.5 - 5.5	± 4	12	-40~125	•	•	•						
74HC165-Q100	8-bit parallel or serial-in/serial-out shift register	2.0 - 6.0	± 5.2	16	-40~125				•		•	•		
74HCT165-Q100	8-bit parallel or serial-in/serial-out shift register; TTL-enabled	4.5 - 5.5	± 4	14	-40~125				•		•	•		
74HC166-Q100	8-bit parallel or serial-in/serial-out shift register	2.0 - 6.0	± 5.2	15	-40~125				•		•			
74HCT166-Q100	8-bit parallel or serial-in/serial-out shift register; TTL-enabled	4.5 - 5.5	± 4	23	-40~125				•					
74HC594-Q100	8-bit serial-in/parallel-out shift register with output storage register	2.0 - 6.0	± 7.8	14	-40~125				•					
74HCT594-Q100	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled	4.5 - 5.5	± 6	15	-40~125				•					
74HC595-Q100	8-bit serial-in/parallel-out shift register with output storage register (3-state)	2.0 - 6.0	± 7.8	16	-40~125				•	•	•	•		
74HCT595-Q100	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	4.5 - 5.5	± 6	25	-40~125				•		•	•		
74HC597-Q100	8-bit parallel or serial-in/parallel-out shift register with parallel input register	2.0 - 6.0	± 5.2	16	-40~125				•		•			
74HCT597-Q100	8-bit parallel or serial-in/parallel-out shift register with parallel input register; TTL-enabled	4.5 - 5.5	± 4	20	-40~125				•					
74HC4094-Q100	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	2.0 - 6.0	± 5.2	15	-40~125				•	•	•			
74HCT4094-Q100	8-bit serial-in/serial or parallel-out shift register with output register; TTL-enabled (3-state)	4.5 - 5.5	± 4	19	-40~125				•	•				
74LV164-Q100	8-bit serial-in/parallel-out shift register	1.0 - 5.5	± 12	12	-40~125	•	•	•						
74LV165-Q100	8-bit parallel or serial-in/serial-out shift register	1.0 - 5.5	± 12	18	-40~125				•		•			
74LV165A-Q100	8-bit parallel or serial-in/serial-out shift register	1.0 - 5.5	± 12	7.5	-40~125				•		•			
74LV4060-Q100	14-stage binary ripple counter with oscillator	1.0 - 5.5	± 6	29	-40~125				•		•			
74LVC594A-Q100	8-bit serial-in/parallel-out shift register with output storage register	1.2 - 5.5	± 24	3.1	-40~125				•		•	•		
74VHC595-Q100	8-bit serial-in/parallel-out shift register with output storage register (3-state)	2.0 - 5.5	± 8	4	-40~125				•		•	•		
74VHCT595-Q100	8-bit serial-in/parallel-out shift register with output storage register; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.8	-40~125				•		•	•		
HEF4014B-Q100	8-bit shift register with synchronous parallel enable	4.5 - 15	± 2.4	40	-40~85				•					

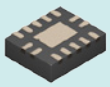
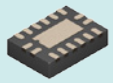
Shift registers (cont.)

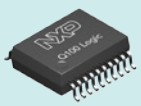
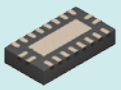
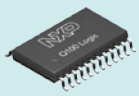
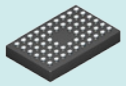
Type number	Description	Features				Package (suffix)								
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT108-1 (D)	SOT402-1 (PW)	SOT762-1 (BQ)	SOT109-1 (D)	SOT338-1 (DB)	SOT403-1 (PW)	SOT763-1 (BQ)	SOT163-1 (D)	SOT360-1 (PW)
HEF4021B-Q100	8-bit shift register with asynchronous parallel load	4.5 - 15	± 2.4	40	-40~85				•		•			
HEF4094B-Q100	8-bit serial-in/serial or parallel-out shift register with output register (3-state)	4.5 - 15	± 2.4	50	-40~85				•		•			
HEF4794B-Q100	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 - 15	-20	45	-40~85				•					
HEF4894B-Q100	12-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 - 15	-20	45	-40~85								•	•
NPIC6C595-Q100	8-bit serial-in/parallel-out shift register with output storage register (3-state)	4.5 - 5.5	-100	90	-40~125				•		•	•		
NPIC6C596-Q100	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 - 5.5	-100	90	-40~125				•		•	•		
NPIC6C596A-Q100	8-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	2.3 - 5.5	-100	90	-40~125				•		•	•		
NPIC6C4894-Q100	12-bit serial-in/serial or parallel-out shift register with output register LED driver (3-state)	4.5 - 5.5	-100	105	-40~125								•	•

Transceivers

Type number	Description	Features				Package (suffix)				
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT163-1 (D)	SOT360-1 (PW)	SOT764-1 (BQ)	SOT362-1 (DGG)	SOT702-1 (EV)
74AHC245-Q100	Octal transceiver (3-state)	2.0 - 5.5	± 8	3.5	-40~125	•	•	•		
74AHCT245-Q100	Octal transceiver; TTL-enabled (3-state)	4.5 - 5.5	± 8	5	-40~125	•	•	•		
74AVC16245-Q100	16-bit transceiver (3-state)	1.2 - 3.6	± 12	2	-40~85				•	
74HC245-Q100	Octal transceiver (3-state)	2.0 - 6.0	± 7.8	7	-40~125	•	•	•		
74HCT245-Q100	Octal transceiver; TTL-enabled (3-state)	4.5 - 5.5	± 6	10	-40~125	•	•	•		
74LVC245A-Q100	Octal transceiver (3-state)	1.2 - 3.6	± 24	2.9	-40~125	•	•	•		
74LVCH245A-Q100	Octal transceiver with bus hold (3-state)	1.2 - 3.6	± 24	2.9	-40~125	•	•	•		
74LVC16245A-Q100	16-bit transceiver (3-state)	1.2 - 3.6	± 24	3	-40~125				•	•
74LVCH16245A-Q100	16-bit transceiver with bus hold (3-state)	1.2 - 3.6	± 24	3	-40~125				•	•

Standard logic packages

Package suffix	D	DB	PW	BQ	D	DB	PW	BQ
	14-pin	14-pin	14-pin	14-pin	16-pin	16-pin	16-pin	16-pin
								
Package	SOT108-1	SOT337-1	SOT402-1	SOT762-1	SOT109-1	SOT338-1	SOT403-1	SOT763-1
Width (mm)	6.00	7.75	6.40	2.50	6.00	7.75	6.40	2.50
Length (mm)	8.65	6.20	5.00	3.00	9.90	6.20	5.00	3.50
Height (mm)	1.75	2.00	1.10	1.00	1.75	2.00	1.10	1.00
Pitch (mm)	1.27	0.65	0.65	0.50	1.27	0.65	0.65	0.50

Package suffix	D	DB	PW	BQ	D	PW	DGG	EV
	20-pin	20-pin	20-pin	20-pin	24-pin	24-pin	48-pin	56-pin
								
Package	SOT163-1	SOT339-1	SOT360-1	SOT764-1	SOT137-1	SOT355-1	SOT362-1	SOT702-1
Width (mm)	10.30	7.75	6.40	2.50	10.30	6.40	8.10	4.50
Length (mm)	12.80	7.20	6.50	4.50	15.40	7.80	12.50	7.00
Height (mm)	2.65	2.00	1.10	1.00	2.65	1.10	1.20	1.00
Pitch (mm)	1.27	0.65	0.65	0.5	1.27	0.65	0.50	0.65

Note: The HEF4000B family uses different package suffixes than the other families. Package suffix D corresponds to HEF4000B package suffix T, DB to TS and PW to TT.

Q100 Mini Logic functions & packages

Mini logic functions are small footprint logic devices with 10 pins or less suitable for use at supply voltage between 1.1 V to 6.0 V. They provide a wide range of functions including analog switches, buffers/inverters, bus switches, decoders/de-multiplexers, multiplexers, flip-flops, gates, configurable logic and level shifters. Q100 Mini logic functions are available in leaded TSSOP and VSSOP packages as well as innovative leadless XSON packages.

Analog switches

Type number	Description	Features					Package (suffix)					
		Configuration	V_{CC} (V)	R_{ON} (Ω)	R_{ON}(FLAT) (Ω)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)
74AHC1G66-Q100	Single-pole, single-throw analog switch	SPST-NO	2.0 - 5.5	40	5	-40~125	•	•				
74AHCT1G66-Q100	Single-pole, single-throw analog switch; TTL-enabled	SPST-NO	4.5 - 5.5	40	5	-40~125	•	•				
74HC1G66-Q100	Single-pole, single-throw analog switch	SPST-NO	2.0 - 9.0	105	23	-40~125	•	•				
74HCT1G66-Q100	Single-pole, single-throw analog switch; TTL-enabled	SPST-NO	4.5 - 5.5	118	23	-40~125	•	•				
74HC2G66-Q100	Dual single-pole, single-throw analog switch	SPST-NO	2.0 - 9.0	105	23	-40~125					•	•
74HCT2G66-Q100	Dual single-pole, single-throw analog switch; TTL-enabled	SPST-NO	4.5 - 5.5	118	23	-40~125					•	•
74LVC1G53-Q100	Single-pole, double-throw analog switch	SPDT-Z	1.65 - 5.5	15	1.5	-40~125					•	•
74LVC1G66-Q100	Single-pole, single-throw analog switch	SPST-NO	1.65 - 5.5	15	1.5	-40~125	•	•				
74LVC1G384-Q100	Single-pole, single-throw analog switch	SPST-NC	1.65 - 5.5	15	1.5	-40~125	•	•				
74LVC1G3157-Q100	Single-pole, double-throw analog switch	SPDT	1.65 - 5.5	15	1.5	-40~125			•	•		
74LVC2G66-Q100	Dual single-pole, single-throw analog switch	SPST-NO	1.65 - 5.5	15	1.5	-40~125					•	•

Bus switches

Type number	Description	Features				Package (suffix)	
		V_{CC} (V)	V_{PASS} (V)	R_{ON} (Ω)	T_{amb} (°C)	SOT96-1 (D)	SOT530-1 (PW)
CBT3306-Q100	Dual bus switch	4.5 - 5.5	3.9	7	-40~85	•	•

Buffers/inverters

Type number	Description	Features				Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)	SOT996-2 (GD)
74AHC1GU04-Q100	Single inverter; unbuffered	2.0 - 5.5	± 8	2.6	-40~125	•	•					
74AHC3GU04-Q100	Triple inverter; unbuffered	2.0 - 5.5	± 8	2.5	-40~125					•	•	
74AHC1G04-Q100	Single inverter	2.0 - 5.5	± 8	3.1	-40~125	•	•					
74AHCT1G04-Q100	Single inverter; TTL-enabled	4.5 - 5.5	± 8	3.4	-40~125	•	•					
74AHC1G07-Q100	Single buffer; open-drain	2.0 - 5.5	8	4.2	-40~125	•	•					
74AHC1G125-Q100	Single buffer/line driver (3-state)	2.0 - 5.5	± 8	3.4	-40~125	•	•					
74AHCT1G125-Q100	Single buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.4	-40~125	•	•					
74AHC1G126-Q100	Single buffer/line driver (3-state)	2.0 - 5.5	± 8	3.4	-40~125	•	•					
74AHCT1G126-Q100	Single buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.4	-40~125	•	•					
74AHC2G125-Q100	Dual buffer/line driver (3-state)	2.0 - 5.5	± 8	3.4	-40~125					•	•	
74AHCT2G125-Q100	Dual buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.4	-40~125					•	•	
74AHC2G126-Q100	Dual buffer/line driver (3-state)	2.0 - 5.5	± 8	3.4	-40~125					•	•	
74AHCT2G126-Q100	Dual buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.4	-40~125					•	•	
74AHC2G241-Q100	Dual buffer/line driver (3-state)	2.0 - 5.5	± 8	3.4	-40~125					•	•	
74AHCT2G241-Q100	Dual buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 8	3.4	-40~125					•	•	
74AHC3G04-Q100	Triple inverter	2.0 - 5.5	± 8	3.1	-40~125					•	•	
74AHCT3G04-Q100	Triple inverter; TTL-enabled	4.5 - 5.5	± 8	3	-40~125					•	•	
74AUP1G04-Q100	Single inverter	1.1 - 3.6	± 1.9	4	-40~125	•	•					
74AUP1G06-Q100	Single inverter; open-drain	1.1 - 3.6	1.9	4.5	-40~125	•						
74AUP1G34-Q100	Single buffer	1.1 - 3.6	± 1.9	3.9	-40~125	•						
74AUP1G125-Q100	Single buffer/line driver (3-state)	1.1 - 3.6	± 1.9	4.3	-40~125	•						
74AUP2GU04-Q100	Dual inverter; unbuffered	1.1 - 3.6	± 1.9	2.3	-40~125			•				
74HC1GU04-Q100	Single inverter; unbuffered	2.0 - 6.0	± 2.6	5	-40~125	•	•					
74HC2GU04-Q100	Dual inverter; unbuffered	2.0 - 6.0	± 5.2	5	-40~125			•	•			
74HC3GU04-Q100	Triple inverter; unbuffered	2.0 - 6.0	± 5.2	6	-40~125					•	•	
74HC1G04-Q100	Single inverter	2.0 - 6.0	± 2.6	7	-40~125	•	•					
74HCT1G04-Q100	Single inverter; TTL-enabled	4.5 - 5.5	± 2.0	8	-40~125	•	•					
74HC1G125-Q100	Single buffer/line driver (3-state)	2.0 - 6.0	± 2.6	9	-40~125	•	•					
74HCT1G125-Q100	Single buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 2.0	10	-40~125	•	•					
74HC2G04-Q100	Dual inverter	2.0 - 6.0	± 5.2	8	-40~125			•	•			
74HCT2G04-Q100	Dual inverter; TTL-enabled	4.5 - 5.5	± 4.0	10	-40~125			•	•			
74HC2G34-Q100	Dual buffer	2.0 - 6.0	± 5.2	9	-40~125			•	•			
74HCT2G34-Q100	Dual buffer; TTL-enabled	4.5 - 5.5	± 4.0	10	-40~125			•	•			
74HC2G125-Q100	Dual buffer/line driver (3-state)	2.0 - 6.0	± 5.2	10	-40~125					•	•	

Buffers/inverters (cont.)

Type number	Description	Features				Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)	SOT996-2 (GD)
74HCT2G125-Q100	Dual buffer/line driver; TTL-enabled (3-state)	4.5 - 5.5	± 4.0	12	-40~125					•	•	
74HC3G04-Q100	Triple inverter	2.0 - 6.0	± 5.2	8	-40~125					•	•	•
74HCT3G04-Q100	Triple inverter; TTL-enabled	4.5 - 5.5	± 4.0	10	-40~125					•	•	•
74HC3G07-Q100	Triple buffer; open-drain	2.0 - 6.0	5.2	9	-40~125					•	•	
74HCT3G07-Q100	Triple buffer; open-drain; TTL-enabled	4.5 - 5.5	4	9	-40~125					•	•	
74HC3G34-Q100	Triple buffer	2.0 - 6.0	± 5.2	9	-40~125					•	•	
74HCT3G34-Q100	Triple buffer; TTL-enabled	4.5 - 5.5	± 4.0	10	-40~125						•	
74LVC1G04-Q100	Single inverter	1.65 - 5.5	± 32	2	-40~125	•	•					
74LVC1G06-Q100	Single inverter; open-drain	1.65 - 5.5	32	2.3	-40~125	•	•					
74LVC1G07-Q100	Single buffer; open-drain	1.65 - 5.5	32	2.2	-40~125	•	•					
74LVC1G34-Q100	Single buffer	1.65 - 5.5	± 32	2	-40~125	•	•					
74LVC1G125-Q100	Single buffer/line driver (3-state)	1.65 - 5.5	± 32	2.1	-40~125	•	•					
74LVC1G126-Q100	Single buffer/line driver (3-state)	1.65 - 5.5	± 32	2	-40~125	•	•					
74LVC1GU04-Q100	Single inverter; unbuffered	1.65 - 5.5	± 32	1.6	-40~125	•	•					
74LVC2G04-Q100	Dual inverter	1.65 - 5.5	± 32	2.7	-40~125			•	•			
74LVC2G06-Q100	Dual inverter; open-drain	1.65 - 5.5	32	2.3	-40~125			•	•			
74LVC2G07-Q100	Dual buffer; open-drain	1.65 - 5.5	32	2.6	-40~125			•	•			
74LVC2G125-Q100	Dual buffer/line driver (3-state)	1.65 - 5.5	± 32	2.3	-40~125					•	•	
74LVC2G240-Q100	Dual inverter/line driver (3-state)	1.65 - 5.5	± 32	2.5	-40~125					•	•	
74LVC2G241-Q100	Dual buffer/line driver (3-state)	1.65 - 5.5	± 32	2.6	-40~125					•	•	
74LVC2GU04-Q100	Dual inverter; unbuffered	1.65 - 5.5	± 32	2.3	-40~125			•	•			
74LVC3G04-Q100	Triple inverter	1.65 - 5.5	± 32	2.7	-40~125					•	•	
74LVC3G07-Q100	Triple buffer; open-drain	1.65 - 5.5	32	2.1	-40~125					•	•	
74LVC3G34-Q100	Triple buffer	1.65 - 5.5	± 32	2.2	-40~125					•	•	

Digital decoders/demultiplexers

Type number	Description	Features				Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT363 (GW)	SOT457 (GV)
74LVC1G18-Q100	1-to-2 demultiplexer (3-state)	1.65 - 5.5	± 32	2.3	-40~125	•	•

Digital multiplexers

Type number	Description	Features				Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT363 (GW)	SOT457 (GV)
74LVC1G157-Q100	Single 2-input multiplexer	1.65 - 5.5	± 32	2.2	-40~125	•	•

Flip-flops

Type number	Description	Features				Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)	SOT996-2 (GD)
74AHC1G79-Q100	Single D-type flip-flop; positive-edge trigger	2.0 - 5.5	± 8	3.5	-40~125	•	•					
74AHCT1G79-Q100	Single D-type flip-flop; positive-edge trigger; TTL-enabled	4.5 - 5.5	± 8	3.5	-40~125	•	•					
74AUP1G175-Q100	Single D flip-flop with reset; positive-edge trigger	1.1 - 3.6	± 1.9	7.4	-40~125			•				
74AUP1G374-Q100	Single D-type flip-flop; positive-edge trigger (3-state)	1.1 - 3.6	± 1.9	7.9	-40~125			•				
74AUP2G79-Q100	Dual D-type flip-flop; positive-edge trigger	1.1 - 3.6	± 1.9	8.5	-40~125						•	
74LVC1G74-Q100	Single D-type flip-flop with set and reset; positive-edge trigger	1.65 - 5.5	± 32	3.5	-40~125					•	•	•
74LVC1G80-Q100	Single D-type flip-flop; positive-edge trigger	1.65 - 5.5	± 32	2.4	-40~125	•	•					
74LVC1G175-Q100	Single D flip-flop with reset; positive-edge trigger	1.65 - 5.5	± 32	3.1	-40~125			•	•			
74LVC2G74-Q100	Single D-type flip-flop with set and reset; positive-edge trigger	1.65 - 5.5	± 32	3.5	-40~125					•	•	

Gates

Type number	Description	Features				Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)
74AHC1G09-Q100	Single 2-input AND gate; open-drain	2.0 - 5.5	± 8	3.2	-40~125	•	•				
74AHC1G00-Q100	Single 2-input NAND gate	2.0 - 5.5	± 8	3.5	-40~125	•	•				
74AHCT1G00-Q100	Single 2-input NAND gate; TTL-enabled	4.5 - 5.5	± 8	3.6	-40~125	•	•				
74AHC1G02-Q100	Single 2-input NOR gate	2.0 - 5.5	± 8	3.2	-40~125	•	•				
74AHCT1G02-Q100	Single 2-input NOR gate; TTL-enabled	4.5 - 5.5	± 8	3.5	-40~125	•	•				
74AHC1G08-Q100	Single 2-input AND gate	2.0 - 5.5	± 8	3.2	-40~125	•	•				
74AHCT1G08-Q100	Single 2-input AND gate; TTL-enabled	4.5 - 5.5	± 8	3.6	-40~125	•	•				
74AHC1G32-Q100	Single 2-input OR gate	2.0 - 5.5	± 8	3.2	-40~125	•	•				
74AHCT1G32-Q100	Single 2-input OR gate; TTL-enabled	4.5 - 5.5	± 8	3.3	-40~125	•	•				
74AHC1G86-Q100	2-input EXCLUSIVE-OR gate	2.0 - 5.5	± 8	3.4	-40~125	•	•				
74AHCT1G86-Q100	2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 - 5.5	± 8	3.5	-40~125	•	•				
74AHC2G00-Q100	Dual 2-input NAND gate	2.0 - 5.5	± 8	3.5	-40~125					•	•
74AHCT2G00-Q100	Dual 2-input NAND gate; TTL-enabled	4.5 - 5.5	± 8	3.6	-40~125					•	•
74AHC2G08-Q100	Dual 2-input AND gate	2.0 - 5.5	± 8	3.2	-40~125					•	•
74AHCT2G08-Q100	Dual 2-Input AND gate; TTL-enabled	4.5 - 5.5	± 8	3.6	-40~125					•	•
74AHC2G32-Q100	Dual 2-input OR gate	2.0 - 5.5	± 8	3.2	-40~125					•	•
74AHCT2G32-Q100	Dual 2-input OR gate; TTL-enabled	4.5 - 5.5	± 8	3.3	-40~125					•	•
74AUP1G02-Q100	Single 2-input NOR gate	1.1 - 3.6	± 1.9	8.2	-40~125	•					
74AUP1G08-Q100	Single 2-input AND gate	1.1 - 3.6	± 1.9	8.2	-40~125	•					
74AUP1G32-Q100	Single 2-input OR gate	1.1 - 3.6	±1.9	7.9	-40~125	•					
74AUP1G86-Q100	Single 2-input EXCLUSIVE-OR gate	1.1 - 3.6	± 1.9	3.3	-40~125	•					
74AUP1T98-Q100	Configurable gate with voltage level translation	2.3-3.6 V	±1.9	8.7	-40~125			•			
74HC1G86-Q100	Single 2-input EXCLUSIVE-OR gate	2.0 - 6.0	± 2.6	9	-40~125	•	•				
74HC1GU04-Q100	Single inverter; unbuffered	2.0 - 6.0	± 2.6	5	-40~125	•					
74HC1G00-Q100	Single 2-input NAND gate	2.0 - 6.0	± 2.6	7	-40~125	•					
74HCT1G00-Q100	Single 2-input NAND gate; TTL-enabled	4.5 - 5.5	± 2	10	-40~125	•	•				
74HC1G02-Q100	Single 2-input NOR gate	2.0 - 6.0	± 2.6	7	-40~125	•	•				
74HCT1G02-Q100	Single 2-input NOR gate; TTL-enabled	4.5 - 5.5	± 2.0	9	-40~125	•	•				
74HC1G08-Q100	Single 2-input AND gate	2.0 - 6.0	± 5.2	7	-40~125	•	•				
74HCT1G08-Q100	Single 2-input AND gate; TTL-enabled	4.5 - 5.5	± 2	11	-40~125	•	•				
74HC1G32-Q100	Single 2-input OR gate	2.0 - 6.0	± 2.6	8	-40~125	•	•				
74HCT1G32-Q100	Single 2-input OR gate; TTL-enabled	4.5 - 5.5	± 2.0	10	-40~125	•	•				
74HC2G00-Q100	Dual 2-input NAND gate	2.0 - 6.0	± 5.6	9	-40~125					•	•

Gates (cont.)

Type number	Description	Features				Package (suffix)					
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)
74HCT2G00-Q100	Dual 2-input NAND gate; TTL-enabled	4.5 - 5.5	± 4	12	-40~125					•	•
74HC2G02-Q100	Dual 2-input NOR gate	2.0 - 6.0	± 5.2	9	-40~125					•	•
74HCT2G02-Q100	Dual 2-input NOR gate; TTL-enabled	4.5 - 5.5	± 4	12	-40~125					•	•
74HC2G08-Q100	Dual 2-input AND gate	2.0 - 6.0	± 5.2	9	-40~125					•	•
74HCT2G08-Q100	Dual 2-Input AND gate; TTL-enabled	4.5 - 5.5	± 4	14	-40~125					•	•
74HC2G32-Q100	Dual 2-input OR gate	2.0 - 6.0	± 5.2	9	-40~125					•	•
74HCT2G32-Q100	Dual 2-input OR gate; TTL-enabled	4.5 - 5.5	± 4.0	13	-40~125					•	•
74HC2G86-Q100	Dual 2-input EXCLUSIVE-OR gate	2.0 - 6.0	± 5.2	9	-40~125					•	•
74HCT2G86-Q100	Dual 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 - 5.5	± 4.0	11	-40~125					•	•
74HCT1G86-Q100	Single 2-input EXCLUSIVE-OR gate; TTL-enabled	4.5 - 5.5	± 2.0	10	-40~125	•	•				
74LVC1G00-Q100	Single 2-input NAND gate	1.65 - 5.5	± 32	2.2	-40~125	•	•				
74LVC1G02-Q100	Single 2-input NOR gate	1.65 - 5.5	± 32	2.1	-40~125	•	•				
74LVC1G08-Q100	Single 2-input AND gate	1.65 - 5.5	± 32	2.1	-40~125	•	•				
74LVC1G11-Q100	Single 3-input AND gate	1.65 - 5.5	± 32	2.6	-40~125			•	•		
74LVC1G32-Q100	Single 2-input OR gate	1.65 - 5.5	± 32	2.1	-40~125	•	•				
74LVC1G38-Q100	Single 2-input NAND gate; open-drain	1.65 - 5.5	32	2.3	-40~125	•	•				
74LVC1G57-Q100	Configurable gate; Schmitt trigger	1.65 - 5.5	± 32	3.8	-40~125			•	•		
74LVC1G58-Q100	Configurable gate; Schmitt trigger	1.65 - 5.5	± 32	3.8	-40~125			•	•		
74LVC1G86-Q100	Single 2-input EXCLUSIVE-OR gate	1.65 - 5.5	± 32	2.4	-40~125	•	•				
74LVC1G332-Q100	Single 3-input OR gate	1.65 - 5.5	± 32	2.6	-40~125			•	•		
74LVC1GX04-Q100	Crystal driver	1.65 - 5.5	± 24	2.8	-40~125			•	•		
74LVC2G02-Q100	Dual 2-input NOR gate	1.65 - 5.5	± 32	2.4	-40~125					•	•
74LVC2G08-Q100	Dual 2-input AND gate	1.65 - 5.5	± 24	2.1	-40~125					•	•
74LVC2G32-Q100	Dual 2-input OR gate	1.65 - 5.5	± 32	2.2	-40~125					•	•
74LVC2G34-Q100	Dual buffer	1.65 - 5.5	± 32	2.2	-40~125			•	•		
74LVC2G86-Q100	Dual 2-input EXCLUSIVE-OR gate	1.65 - 5.5	± 32	2.3	-40~125					•	•

Latches/registered drivers

Type number	Description	Features				Package (suffix)
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT363 (GW)
74AUP1G373-Q100	single D-type transparent latch (3-state)	1.1 - 3.6	±1.9	8.5	-40~125	•

Multivibrators

Type number	Description	Features				Package (suffix)	
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT505-2 (DP)	SOT765-1 (DC)
74LVC1G123-Q100	single retriggerable monostable multivibrator	1.65 - 5.5	± 32	3.5	-40~125	•	•

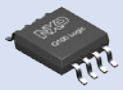
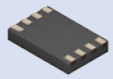
Schmitt triggers

Type number	Description	Features				Package (suffix)						
		V_{CC} (V)	I_O (mA)	t_{pd} (ns)	T_{amb} (°C)	SOT353-1 (GW)	SOT753 (GV)	SOT363 (GW)	SOT457 (GV)	SOT505-2 (DP)	SOT765-1 (DC)	SOT996-2 (GD)
74AHC1G14-Q100	Single inverter Schmitt trigger	2.0 - 5.5	± 8	3.2	-40~125	•	•					
74AHCT1G14-Q100	Single inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 8	4.1	-40~125	•	•					
74AHC3G14-Q100	Triple inverter Schmitt trigger	2.0 - 5.5	± 8	3.2	-40~125					•	•	•
74AHCT3G14-Q100	Triple inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 8	4.1	-40~125					•	•	•
74HC1G14-Q100	Single inverter Schmitt trigger	2.0 - 6.0	± 2.6	10	-40~125	•	•					
74HCT1G14-Q100	Single inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 2.0	15	-40~125	•	•					
74HC2G14-Q100	Dual inverter Schmitt trigger	2.0 - 6.0	± 5.2	16	-40~125			•	•			
74HCT2G14-Q100	Dual inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 4.0	21	-40~125			•	•			
74HC2G17-Q100	Dual buffer Schmitt trigger	2.0 - 6.0	± 5.2	12	-40~125			•	•			
74HCT2G17-Q100	Dual buffer Schmitt trigger; TTL-enabled	4.5 - 5.5	± 4.0	21	-40~125			•	•			
74HC3G14-Q100	Triple inverter Schmitt trigger	2.0 - 6.0	± 5.2	16	-40~125					•	•	
74HCT3G14-Q100	Triple inverter Schmitt trigger; TTL-enabled	4.5 - 5.5	± 4.0	21	-40~125					•	•	
74LVC1G14-Q100	Single inverter Schmitt trigger	1.65 - 5.5	± 32	3	-40~125	•	•					
74LVC1G17-Q100	Single buffer Schmitt trigger	1.65 - 5.5	± 32	3	-40~125	•	•					
74LVC2G14-Q100	Dual inverter Schmitt trigger	1.65 - 5.5	± 32	3.9	-40~125			•	•			
74LVC2G17-Q100	Dual buffer Schmitt trigger	1.65 - 5.5	± 32	3.6	-40~125			•	•			
74LVC3G17-Q100	Triple buffer Schmitt trigger	1.65 - 5.5	± 32	3.6	-40~125					•	•	

Level shifters/translators

Type number	Description	Features				Package (suffix)				
		V_{CC}(A) (V)	V_{CC}(B) (V)	I_O (mA)	T_{amb} (°C)	SOT353-1 (GW)	SOT363 (GW)	SOT505-2 (DP)	SOT765-1 (DC)	SOT996-2 (GD)
74AUP1T34-Q100	Single dual supply translating buffer	1.1 - 3.6	1.1 - 3.6	± 1.9	-40~125	•				
74AVC1T45-Q100	Single dual-supply voltage level translating transceiver (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125		•			
74AVC2T45-Q100	Dual-bit dual-supply voltage level translating transceiver (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125			•	•	•
74AVCH1T45-Q100	Single dual-supply voltage translating transceiver with bus hold (3-state)	0.8 - 3.6	0.8 - 3.6	± 12	-40~125		•			
74LVC1T45-Q100	Single dual-supply voltage level translating transceiver (3-state)	1.2 - 5.5	1.2 - 5.5	± 24	-40~125		•			
74LVCH1T45-Q100	Single dual-supply voltage translating transceiver with bus hold (3-state)	1.2 - 5.5	1.2 - 5.5	± 24	-40~125		•			
74LVC2T45-Q100	Dual-bit dual-supply voltage level translating transceiver (3-state)	1.2 - 5.5	1.2 - 5.5	± 24	-40~125				•	
74LVCH2T45-Q100	Dual-bit dual-supply voltage level translating transceiver with bus hold (3-state)	1.2 - 5.5	1.2 - 5.5	± 24	-40~125				•	

Mini Logic packages

Package suffix	GW	GV	GW	GV	D	DP	PW	DC	GD
	5-pin	5-pin	6-pin	6-pin	8-pin	8-pin	8-pin	8-pin	8-pin
									
Package	SOT353-1	SOT753	SOT363	SOT457	SOT96-1	SOT505-2	SOT530-1	SOT765-1	SOT996-2
Width (mm)	2.10	2.75	2.10	2.75	6.00	4.00	3.00	3.10	3.00
Length (mm)	2.00	2.90	2.00	2.90	4.90	3.00	6.40	2.00	2.00
Height (mm)	1.00	1.00	1.00	1.00	1.75	1.10	1.10	1.00	0.50
Pitch (mm)	0.65	0.95	0.65	0.95	1.27	0.65	0.65	0.50	0.50

Packages

Industry-leading size, performance, and selection NXP is a recognized leader in packaging technology and has, over the years, driven the evolution to smaller, higher-performance formats. We were one of the first to offer leadless packages, and continue to break new ground with unique options like the Diamond package, the world's smallest general-purpose logic package. Delivering industry firsts like the Diamond package underscores NXP's commitment to leadership, innovation, and understanding of a market that is driven by the need for smaller, cheaper, more reliable solutions.

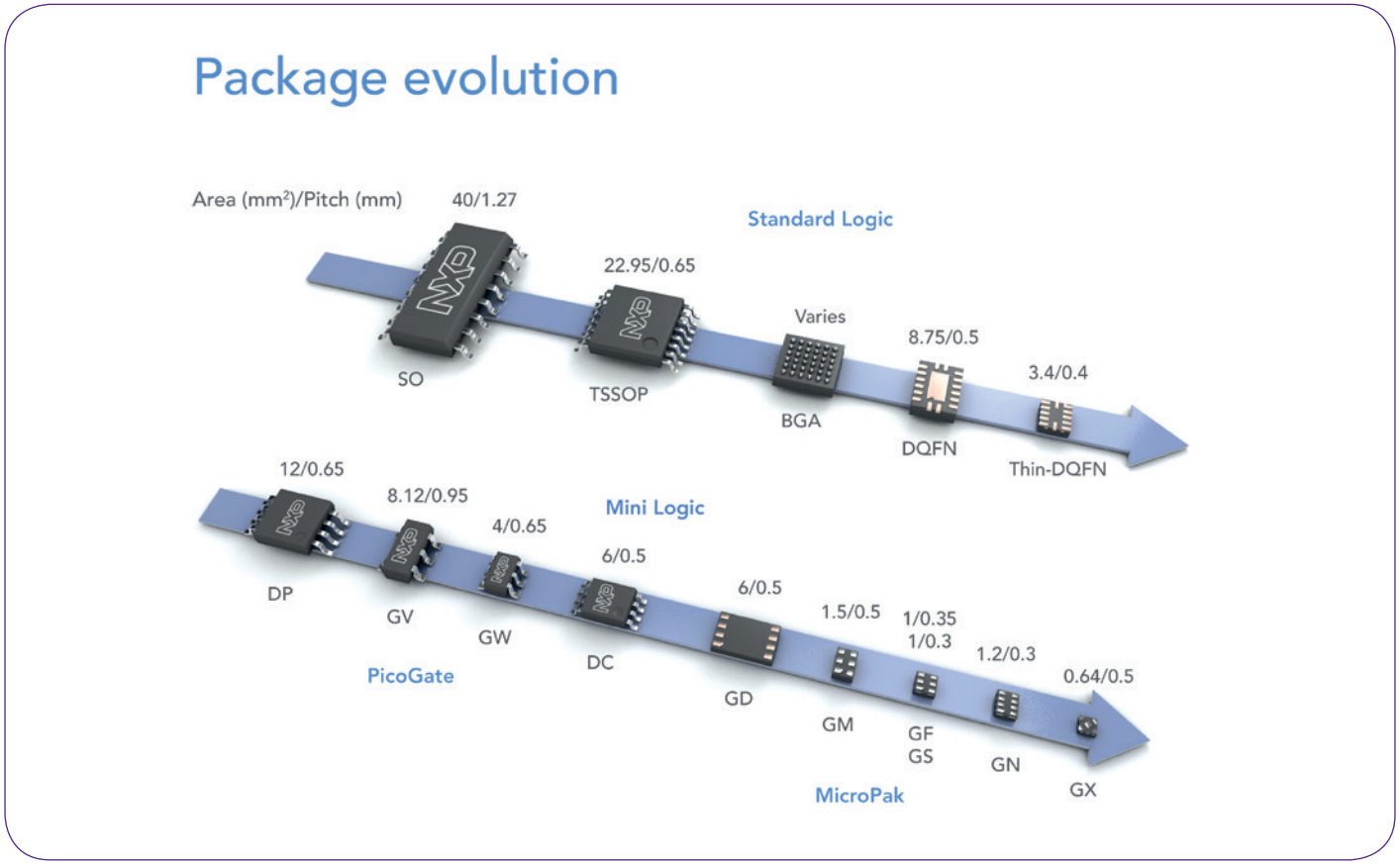
Superior selection

We deliver improved electrical and mechanical performance, smaller size, higher board-level reliability, and lower cost. We support wider temperature ranges (-40 to +125 °C), and offer packages that are automotive qualified according to the AEC-Q100 standard. Our roadmap guides the way to the lowest profile and the smallest pitch.

Support for legacy formats

We may have our eye on the future of packaging, but we also understand the importance of maintaining technologies for as long as they're needed. We know that larger packages, such as SO and TSSOP, still have their place in some designs, and continue to support these tried-and-true solutions.

The journey to smaller formats



The leadless advantage

Today's ultra-compact designs can be a challenge when it comes to squeezing more functionality into a smaller space. Tiny leadless packages can deliver a significant advantage here – with options like DQFN, MicroPak, and Diamond packages offering a smaller footprint with improved mechanical performance.

Leadless packages use pads instead of leads. The pads present a bigger solderable area, so they create a stronger bond with the PCB. The result is a design that is more compact, and also more durable. NXP's DQFN, MicroPak, and Diamond packages perform better in mechanical tests like pull, shear, drop, and bend.

The NXP portfolio includes more than 50 leadless packages, and all are qualified for use in automotive-grade environments. Our LVC, AUP, and AXP logic functions are available in leadless DQFN, MicroPak, and Diamond packages, so it's easy to find the right mix of features, footprint, and cost.

When transitioning to leadless formats, consider the following guidelines:

- For gates, octals, and other logic functions with 10 or more pins, choose the DQFN package. It uses the same die as a TSSOP, but the footprint is up to 76 percent smaller.
- For single-, dual-, and triple-gate functions, which typically use fewer than 10 pins, choose the MicroPak package. It uses the same die as a PicoGate, but the footprint is up to 62 percent smaller.

Recommended replacements for leaded packages

Leaded package	Leadless equivalent	Space savings	Best for functions of
TSSOP	DQFN	Up to 76% smaller	10+ pins
PicoGate	MicroPak	Up to 62% smaller	6 to 10 pins
	Diamond	25% smaller than smallest MicroPak (XSON6)	5 pins

Environmental compliance

Respect for the environment is one of the guiding principles of the NXP Sustainability Policy. Our ongoing commitment to excellence in this area means we continuously move toward best-in-class environmental standards, and supply products that use fewer hazardous or restricted substances and can be recycled or disposed of in an environmentally sound way.

Our products comply with the following:

- European Union Restriction on Hazardous Substances (RoHS) directive
- End of Life Vehicle (ELV) directive
- China RoHS

NXP was one of the earliest semiconductor companies to address environmental concerns over packaging, and we have worked quickly to reduce or eliminate the presence of lead, mercury, chromium, and poly-brominated compounds. We follow the guidelines for compliance with environmental directives, such as RoHS, and go beyond the baseline requirements by reducing the limits of antimony oxides (Sb_2O_3, Sb_2O_5), as well as chlorinated and brominated flame retardants. Our "Dark Green" packages are RoHS compliant and also free of halogen and antimony.

Our Dark Green products have less impact on the environment and, as an added bonus, are more resistant to moisture. Dark Green packages don't require dry-pack processing, which involves drying the package and sealing it in plastic, and this delivers an added saving on energy and resources. The latest Dark Green products also use smaller ICs, so they can be housed in smaller packages. The result is lower cost, fewer materials, lower power consumption and, of course, a reduced environmental footprint.

Definitions of Green and Dark Green

Green = RoHS compliant	
Substance(s)	**Limit**
Pb	< 1000 ppm
Hg, Cr6+, PBB, PBDE	< 1000 ppm
Cd	< 100 ppm

Dark Green = RoHS compliant and free of antimony and halogen	
Substances	**Limit**
Antimony oxides (Sb_2O_3, Sb_2O_5)	< 900 ppm
Chlorinated and brominated flame retardants	$\sum$ < 900 ppm

Note: substances above are not intentionally added, but might be present as an impurity with an upper limit according to the listed values. The plastic materials are classified according to UL94V-0.

Online access to all chemical contents

We were the very first to list all the chemical contents in our products on an easy-to-access web page that also shows compliance with legislative requirements (www.nxp.com/chemical-content/search/). Search results can be downloaded to an Excel or Zip file.

Package selection matrix

	Width (mm)	Pitch (mm)	Suffix	5	6	8	10	12	14	16	20	24	28	48	56	60	96/144
SOIC	3.9	1.27	D / T						SOT108-1	SOT109-1							
	7.5	1.27	D / T								SOT163	SOT137-1	SOT136-1				
SSOP	3.9	0.635	DS / DK							SOT519-1	SOT724-1	SOT556-1					
	5.3	0.65	DB						SOT337-1	SOT338-1	SOT339-1	SOT340-1	SOT341-1				
	7.5	0.635	DL											SOT370-1	SOT371-1		
TSOP	2.8	0.95	GV	SOT753	SOT457												
TSSOP	2.1	0.65	GW	SOT353	SOT363												
	4.4	0.65	PW / TT						SOT402-1	SOT403-1	SOT360-1	SOT355-1	SOT361-1				
	6.1	0.5	DGG											SOT362-1	SOT364-1		
DQFN	2.5	0.5	BQ/ BX						SOT762-1	SOT763-1	SOT764-1						
	3.5	0.5	BQ									SOT815-1					
HUQFN	4	0.5	BX													SOT1025-1	
TVSOP	4.4	0.4	DGV											SOT480-1	SOT481-2		
LFBGA	5.5	0.8	BC														SOT536-1
VFBGA	4.5	0.65	EV												SOT702-1		
XSON	0.8	0.5	GX	SOT1226													
	1.0	0.5	GM/ GT		SOT886	SOT833											
	1.0	0.35	GS		SOT1202	SOT1203											
	1.0	0.3	GN		SOT1115	SOT1116											
	2	0.5	GD			SOT996											
	1	0.35	GF		SOT891		SOT1081										
	1	0.35	DP			SOT1089											
XQFN	1.6	0.5	GM			SOT902	SOT1049	SOT1174									
	1.7	0.5	GU							SOT1161							

Nomenclature

NXP's naming convention embeds the package type in the product number. Our nomenclature diagrams list all items alphabetically.

Nomenclature for standard logic functions

74 XXX XXX XXX

Logic family	Function number	Package type	
AHC(T)		BQ	DQFN
ALVC		BX	DQFN
ALVT		D	SO
AUP		DB	SSOP
AVC(M)		DC	VSSOP
CBT(D)		DG	TSSOP
CBTLV(D)		DGG	TSSOP
HC(T)		DL	SSOP
HEF4000B		DP	TSSOP
LV		FC	BGA
LVC		EV	BGA
LVT		GU	DQFN
NPIC		P	TSSOP
VHC(T)		T	SO
XC7		TS	SSOP
		TT	TSSOP

Nomenclature for mini logic functions

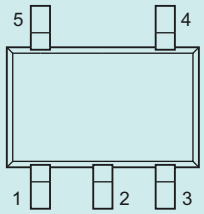
74 XXX XG XT XXX XXX

Logic family	Gate format	Function number	Package type	
AHC(T)	1G Single-gate		DC	PicoGate
AUP	2G Dual-gate		DP	PicoGate
AVC(M)	3G Triple-gate		GD	MicroPak
AXP			GF	MicroPak
CBT(D)	**Translator format**		GM	MicroPak
CBTLV(D)	1T Single-translator		GN	MicroPak
HC(T)	2T Dual-translator		GS	MicroPak
LVC	3T Triple-translator		GT	MicroPak
XC7	4T Quad-translator		GV	PicoGate
			GW	PicoGate
			GX	MicroPak

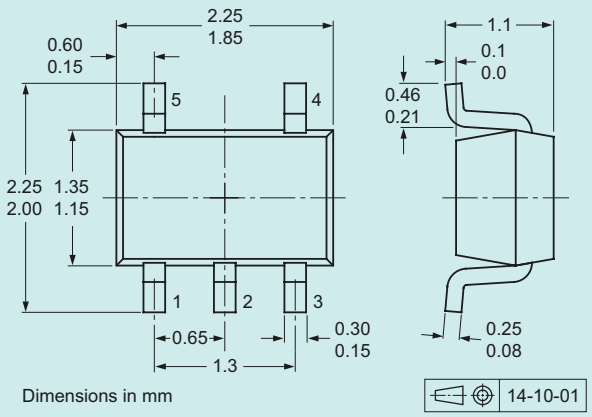
Package diagrams

SOT353 GW

Pinout

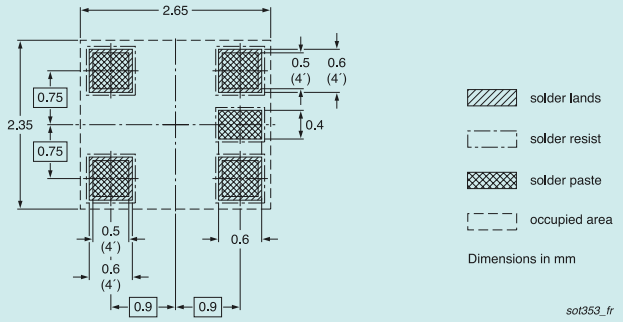


Package dimensions



Dimensions in mm

Solder footprint

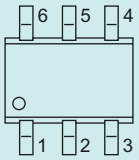


Dimensions in mm

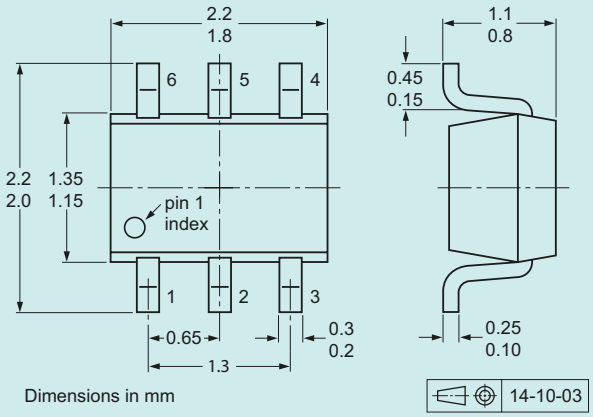
sot353_fr

SOT363 GW

Pinout

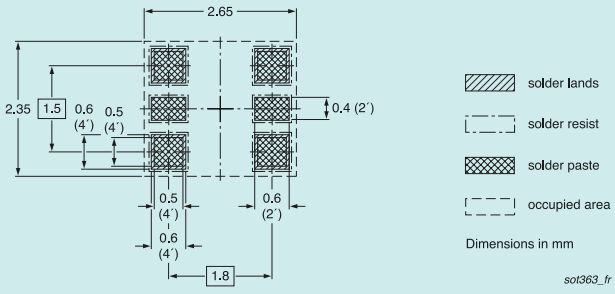


Package dimensions



Dimensions in mm

Solder footprint

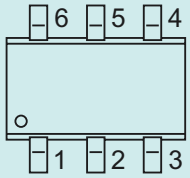


Dimensions in mm

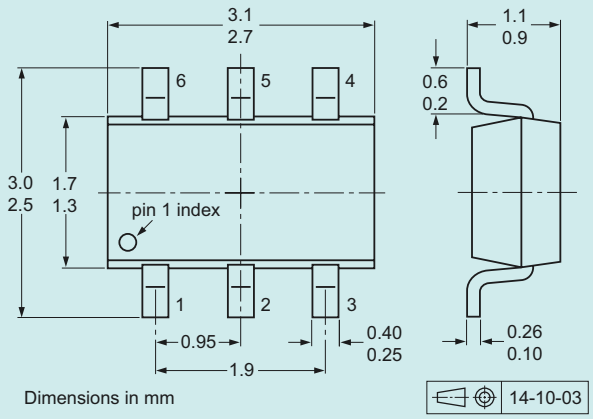
sot363_fr

SOT457 GV

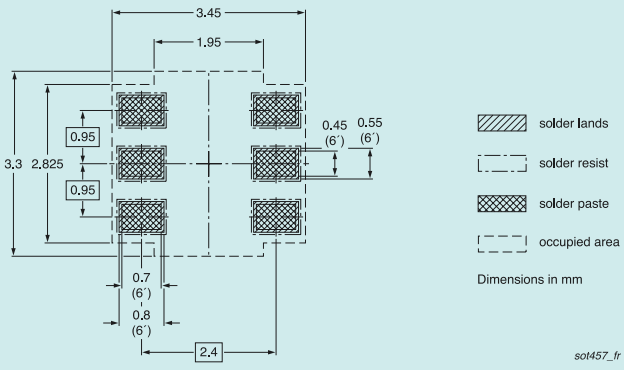
Pinout



Package dimensions

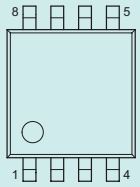


Solder footprint

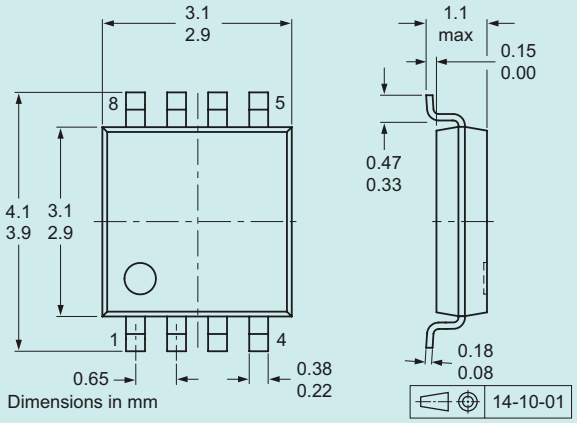


SOT505-2 DP

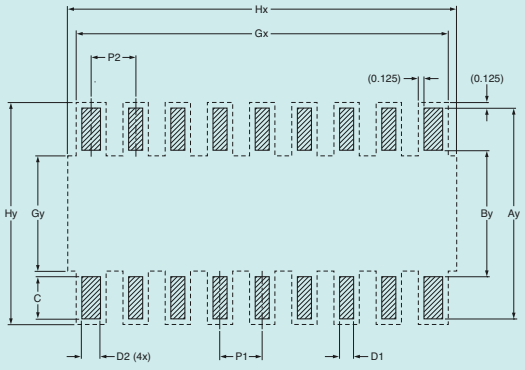
Pinout



Package dimensions

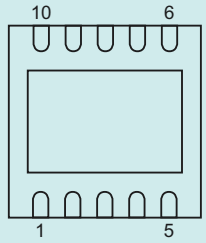


Solder footprint

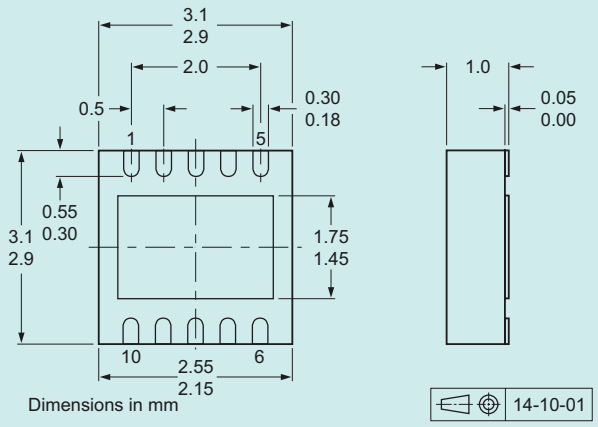


SOT650-1 TK

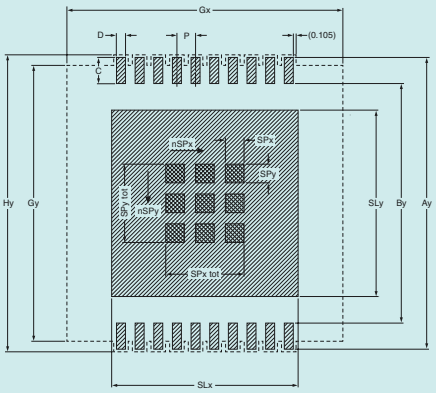
Pinout



Package dimensions

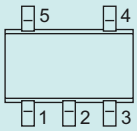


Solder footprint

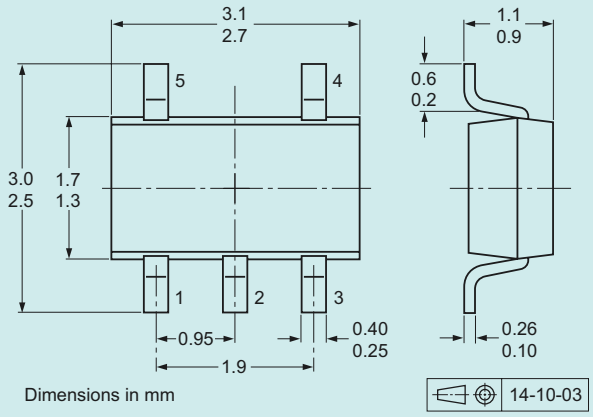


SOT753-1 GV

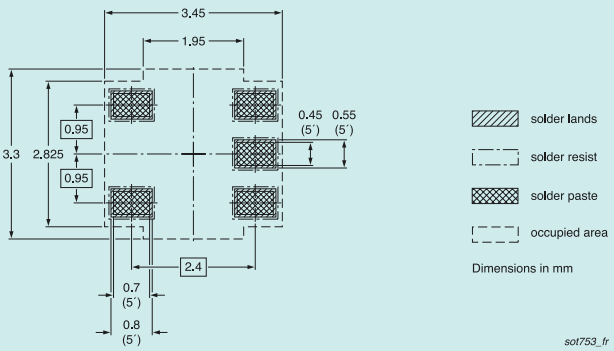
Pinout



Package dimensions

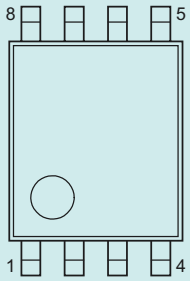


Solder footprint

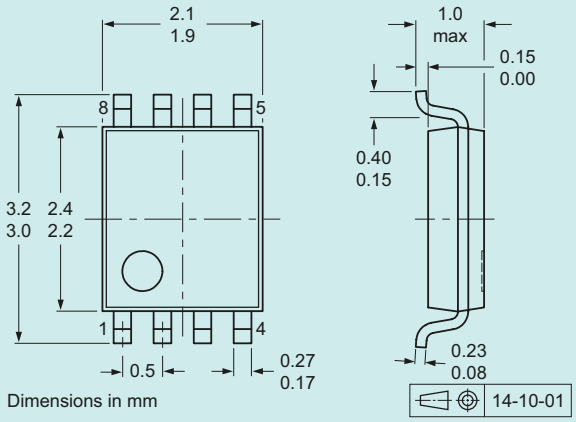


SOT765-1 DC

Pinout

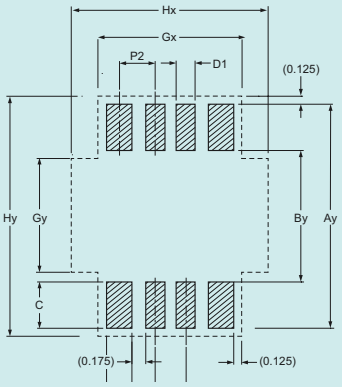


Package dimensions



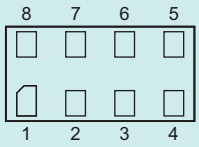
Dimensions in mm

Solder footprint

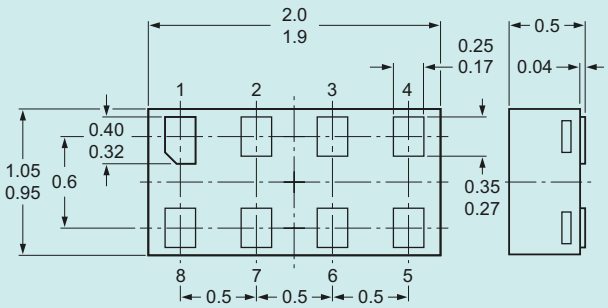


SOT833-1 GT

Pinout

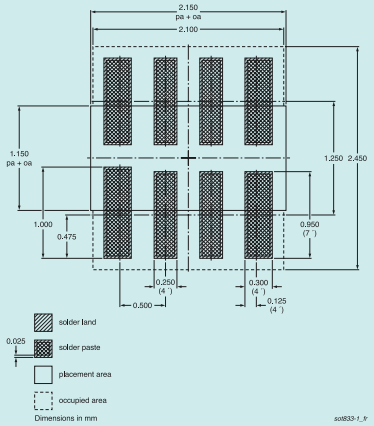


Package dimensions



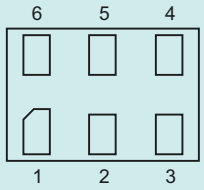
Dimensions in mm

Solder footprint

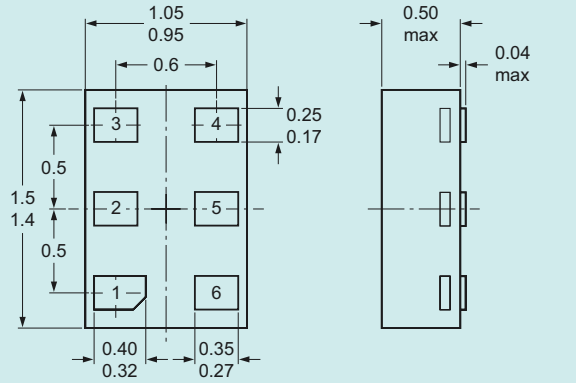


SOT886 GM

Pinout



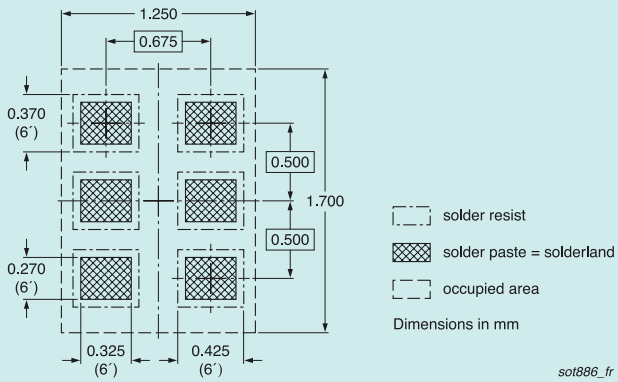
Package dimensions



Dimensions in mm

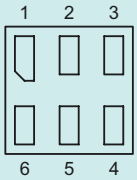
14-10-03

Solder footprint

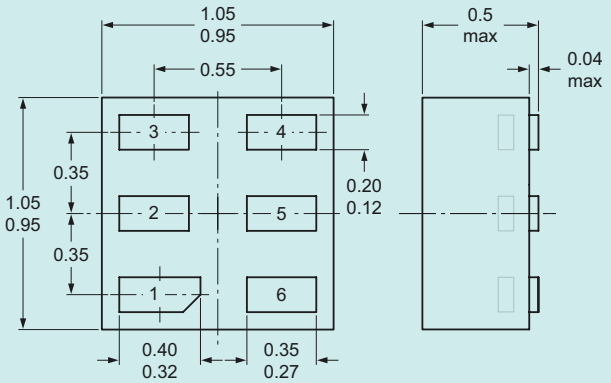


SOT891 GF

Pinout



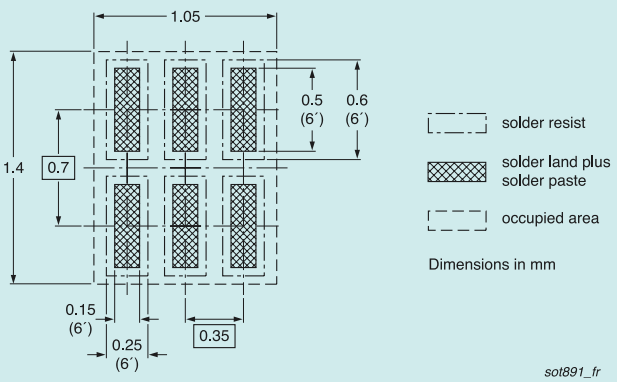
Package dimensions



Dimensions in mm

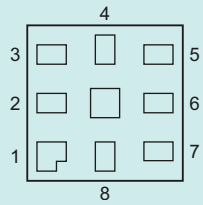
14-10-03

Solder footprint

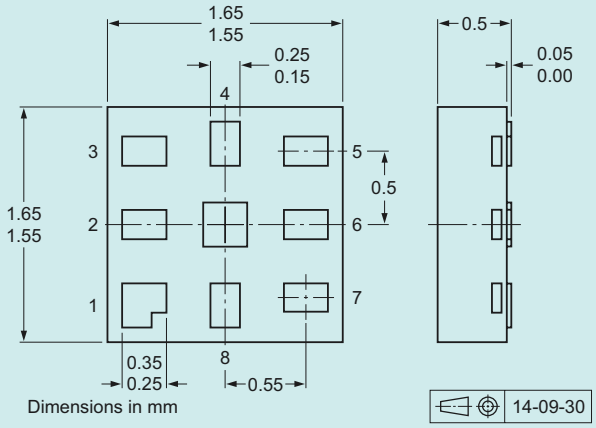


SOT902-2 GM

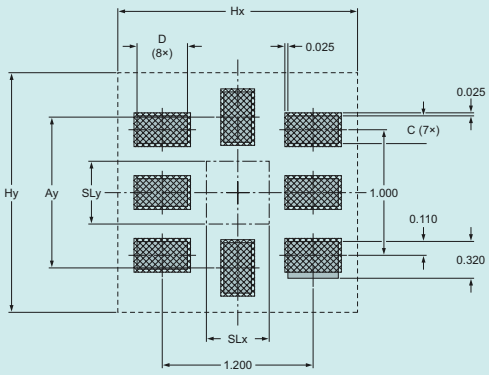
Pinout



Package dimensions

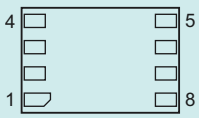


Solder footprint

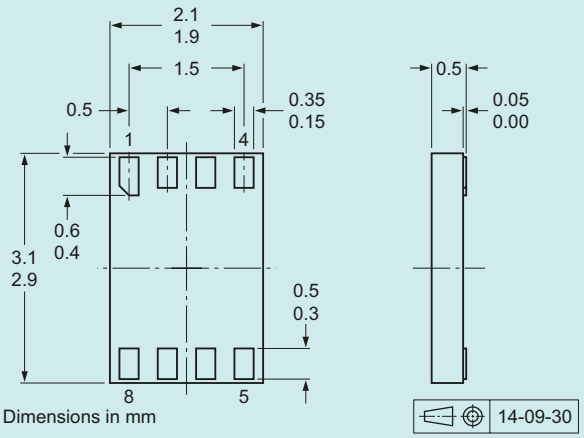


SOT996 GD

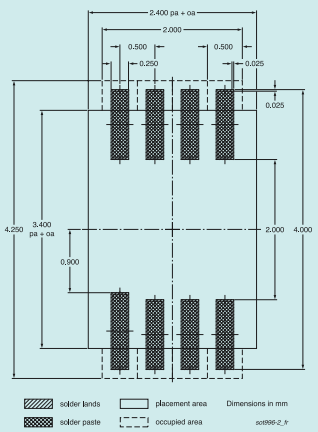
Pinout



Package dimensions

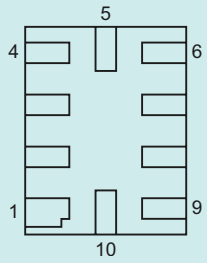


Solder footprint

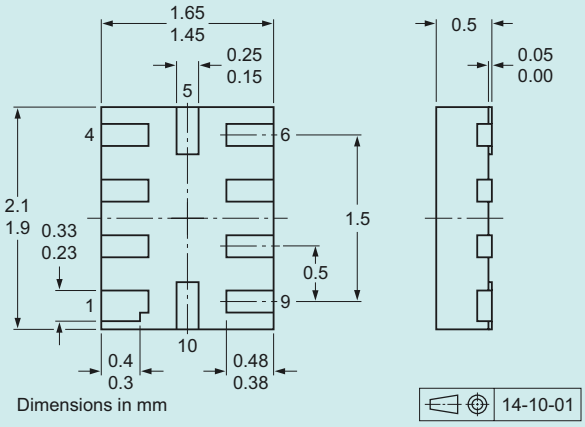


SOT1049-3 GM

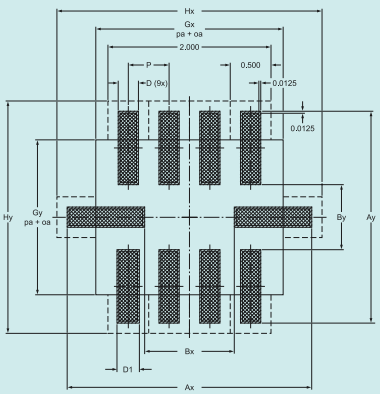
Pinout



Package dimensions

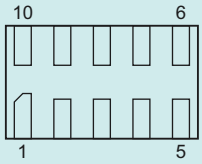


Solder footprint

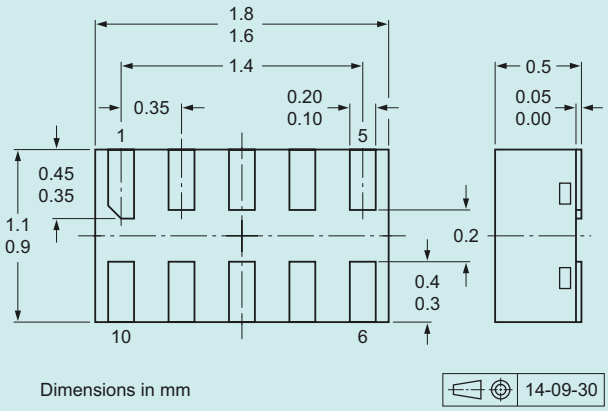


SOT1081-1/2 GF

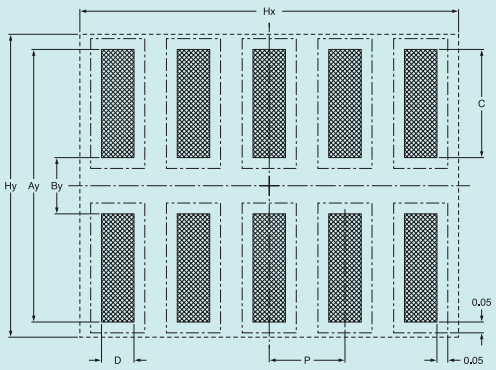
Pinout



Package dimensions

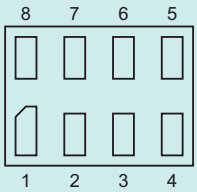


Solder footprint

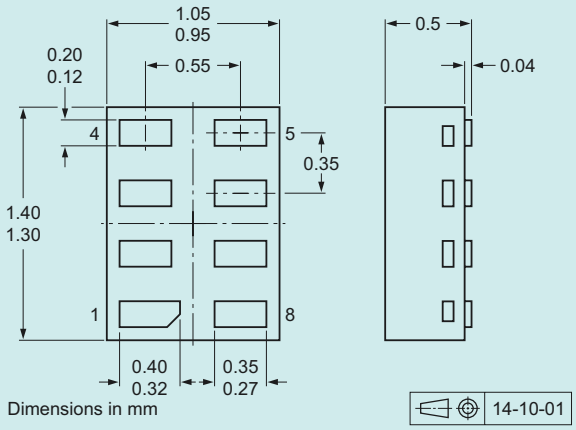


SOT1089 GF

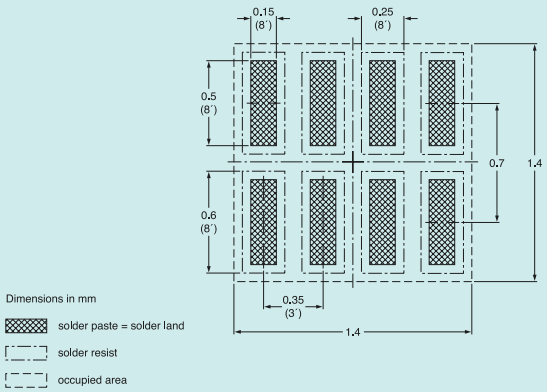
Pinout



Package dimensions

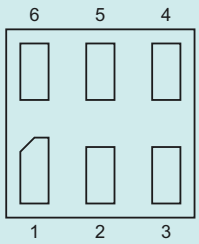


Solder footprint

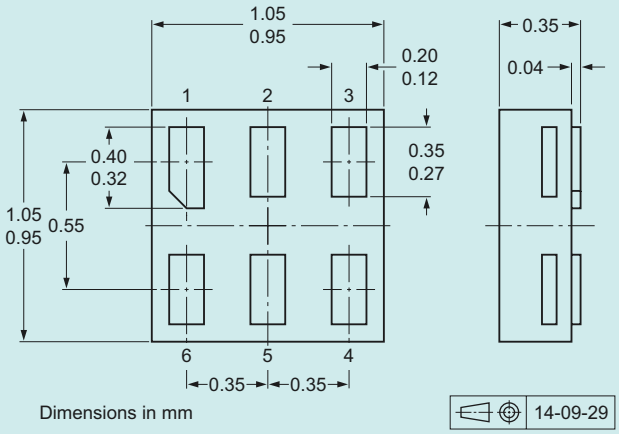


SOT1202 GS

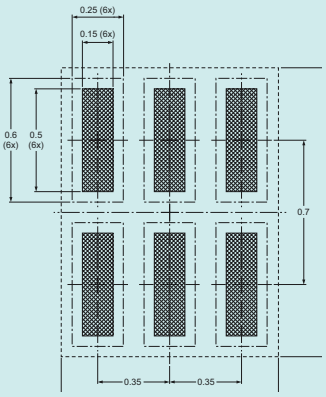
Pinout



Package dimensions

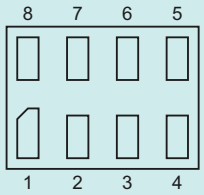


Solder footprint

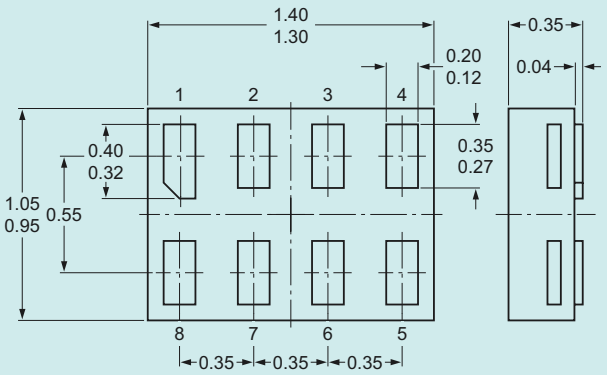


SOT1203 GS

Pinout



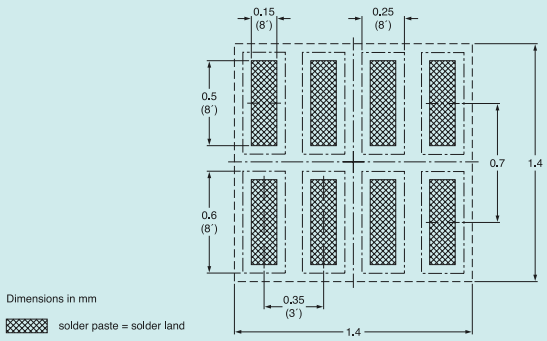
Package dimensions



Dimensions in mm

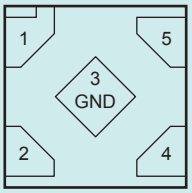
14-09-30

Solder footprint



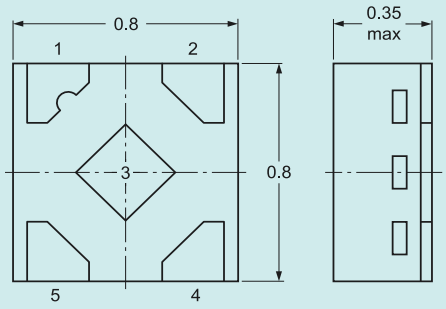
SOT1226 GX

Pinout



aaa-018998

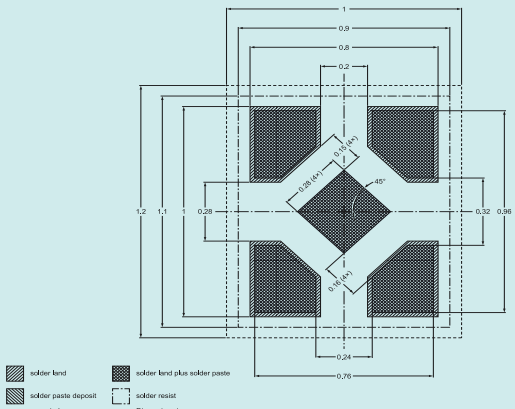
Package dimensions



Dimensions in mm

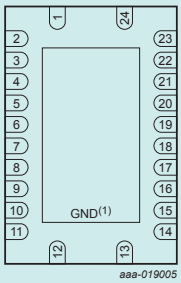
15-05-27

Solder footprint

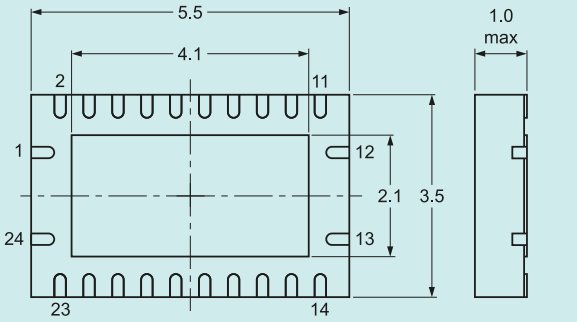


SOT815-1 BQ

Pinout



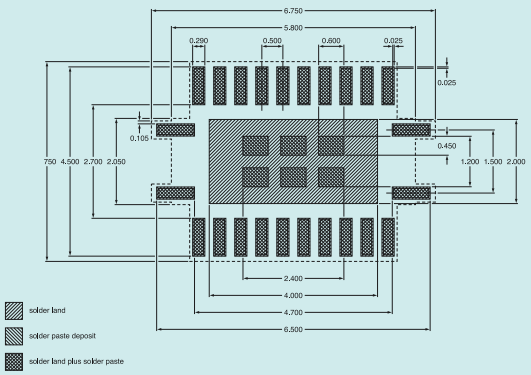
Package dimensions



Dimensions in mm

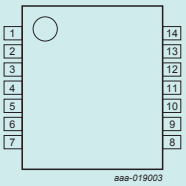
15-05-26

Solder footprint

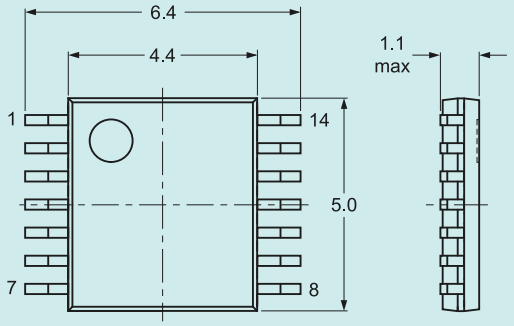


SOT402-1 PW

Pinout



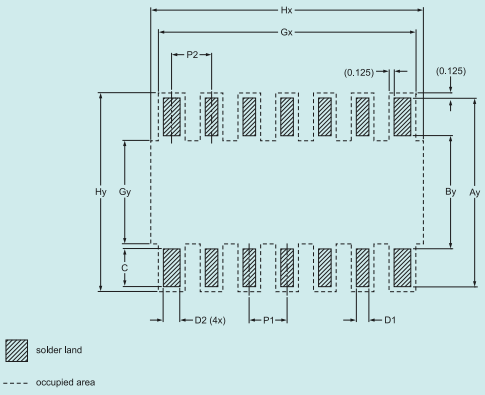
Package dimensions



Dimensions in mm

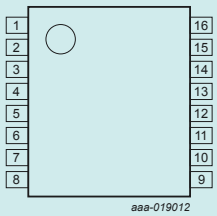
15-05-27

Solder footprint

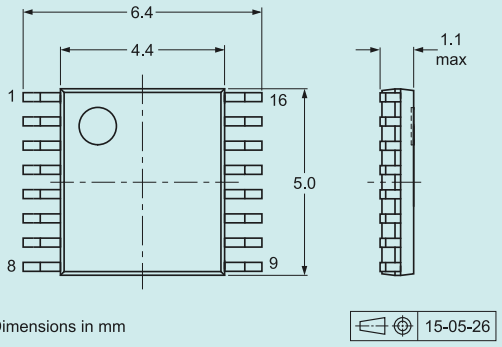


SOT403-1 PW

Pinout

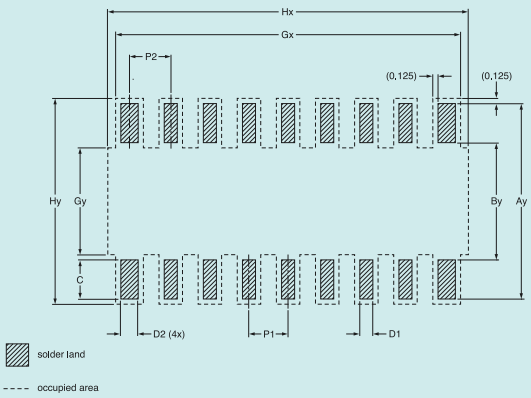


Package dimensions



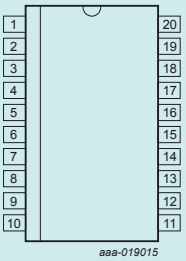
Dimensions in mm

Solder footprint

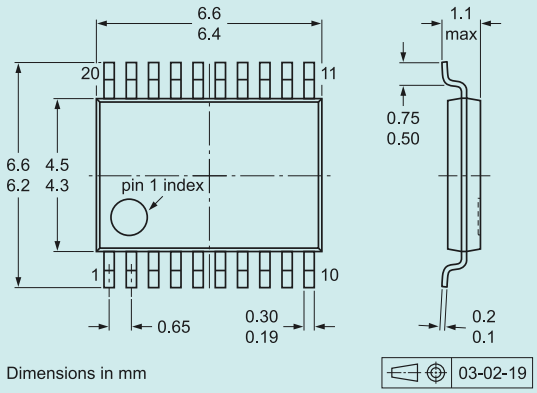


SOT360-1 PW

Pinout

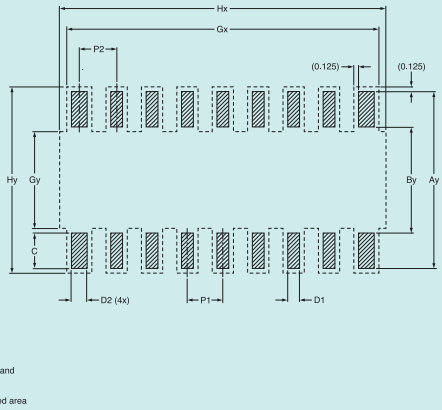


Package dimensions



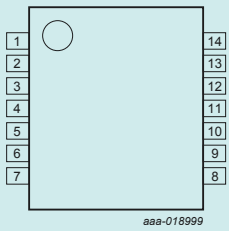
Dimensions in mm

Solder footprint

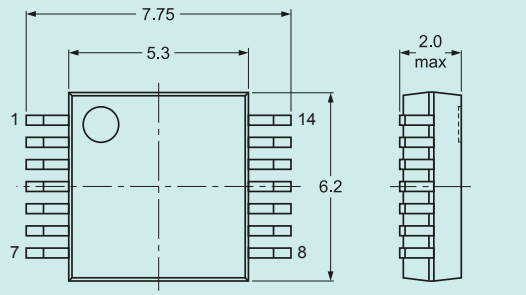


SOT337-1 DB

Pinout



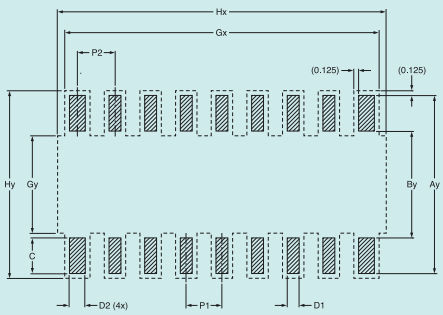
Package dimensions



Dimensions in mm

15-05-26

Solder footprint

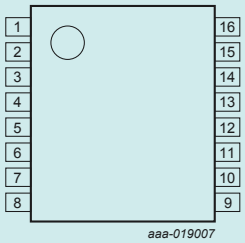


solder land

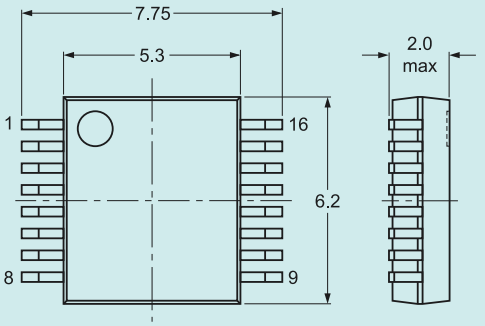
occupied area

SOT338-1 DB

Pinout



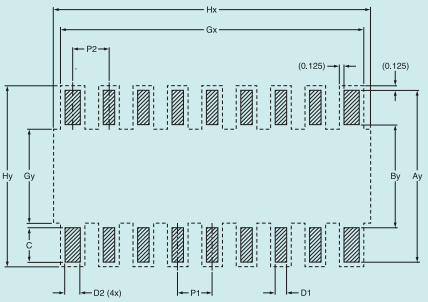
Package dimensions



Dimensions in mm

15-05-27

Solder footprint

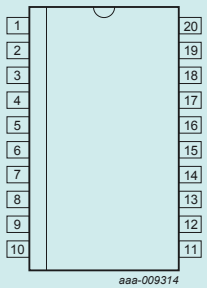


solder land

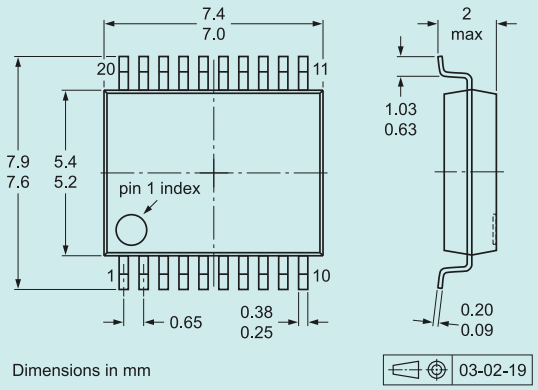
occupied area

SOT339-1 DB

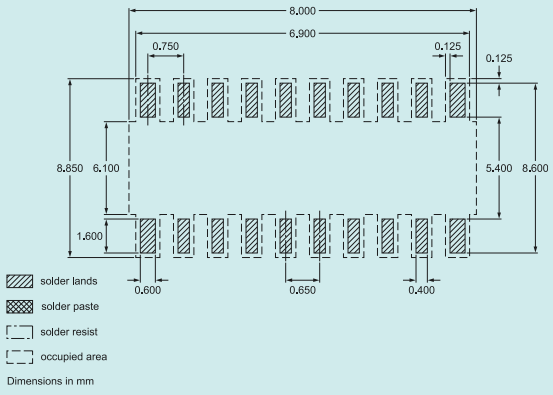
Pinout



Package dimensions

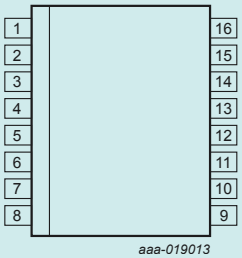


Solder footprint

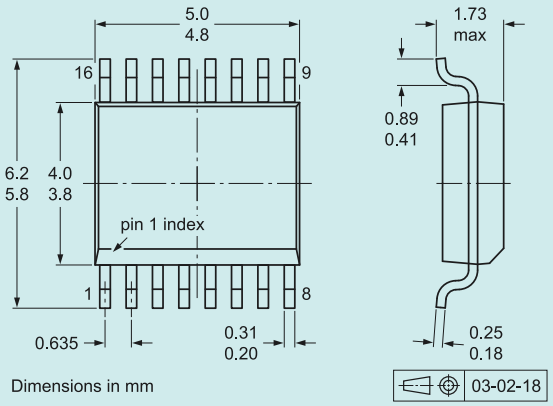


SOT519-1 DS

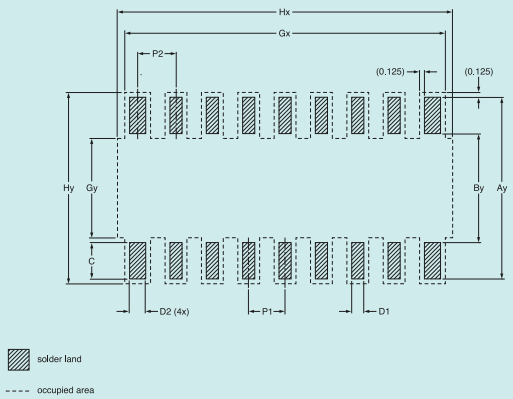
Pinout



Package dimensions

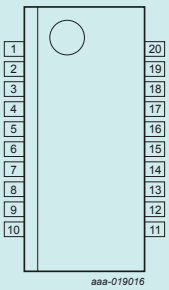


Solder footprint

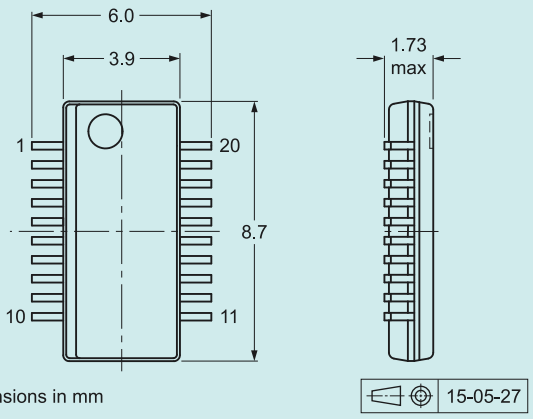


SOT724-1 DS

Pinout

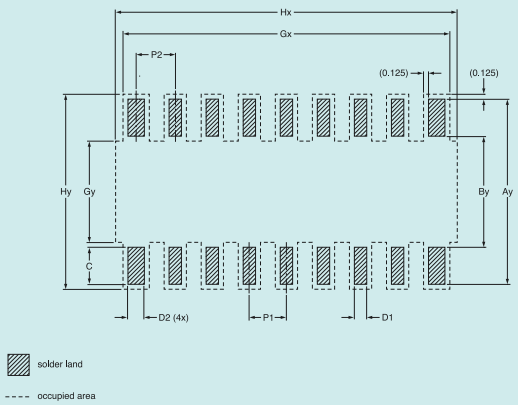


Package dimensions



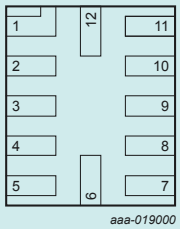
Dimensions in mm

Solder footprint

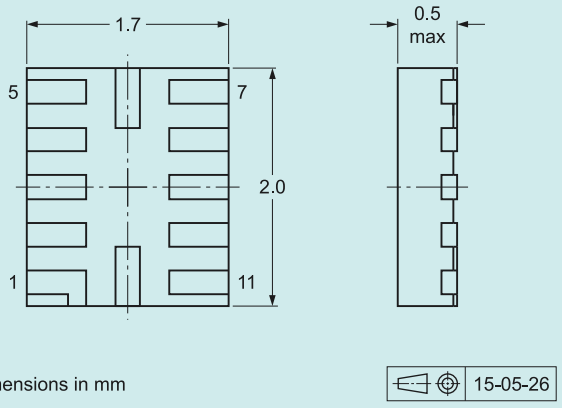


SOT1174 GM

Pinout

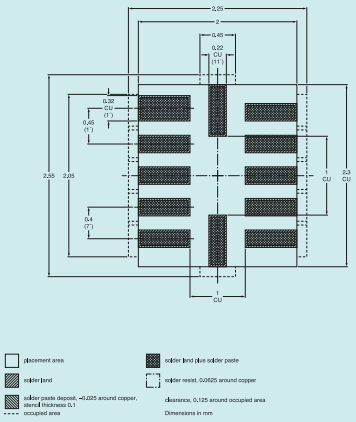


Package dimensions



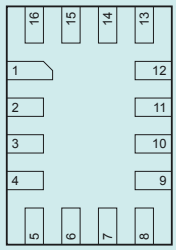
Dimensions in mm

Solder footprint

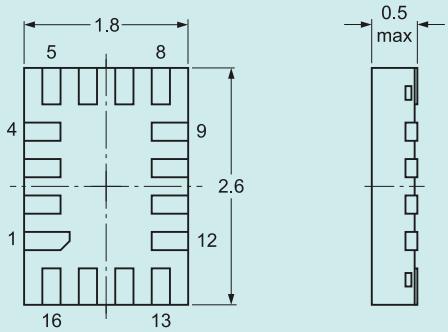


SOT1161 GU

Pinout



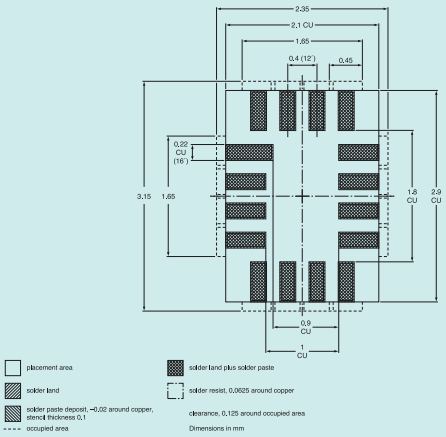
Package dimensions



Dimensions in mm

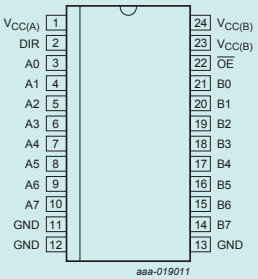
15-05-27

Solder footprint

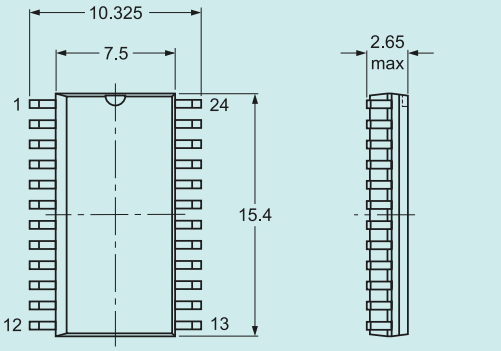


SOT137-1 D

Pinout



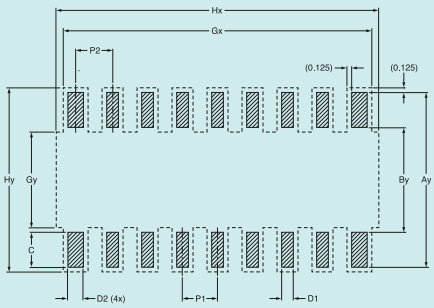
Package dimensions



Dimensions in mm

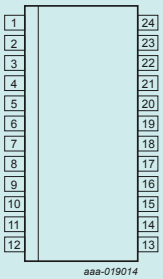
15-05-26

Solder footprint

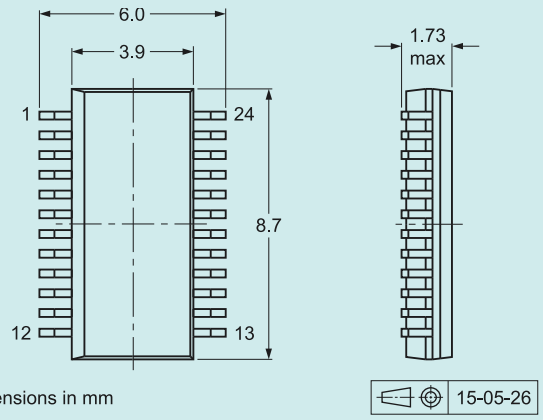


SOT556-1 DK

Pinout

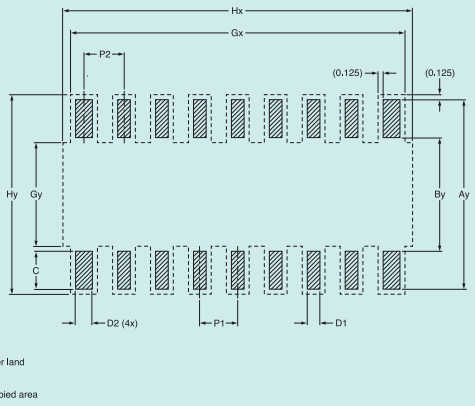


Package dimensions



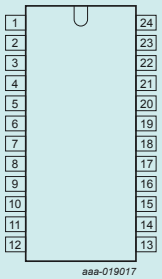
Dimensions in mm

Solder footprint

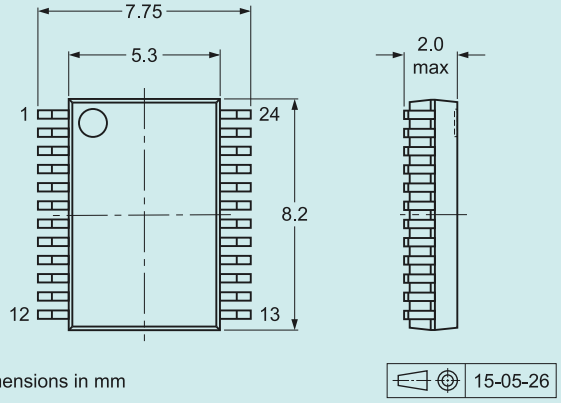


SOT340-1 DB

Pinout

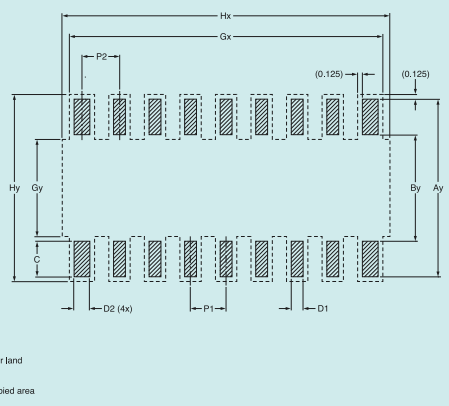


Package dimensions



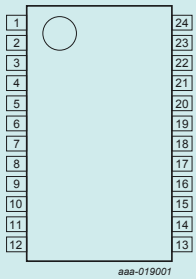
Dimensions in mm

Solder footprint

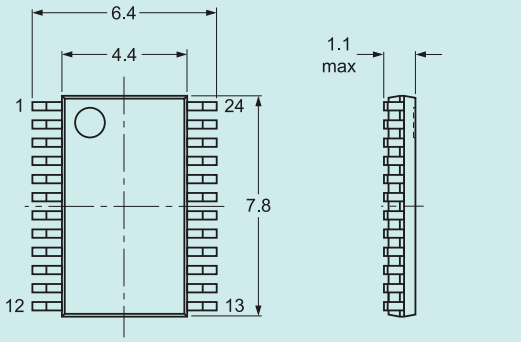


SOT355-1 PW

Pinout



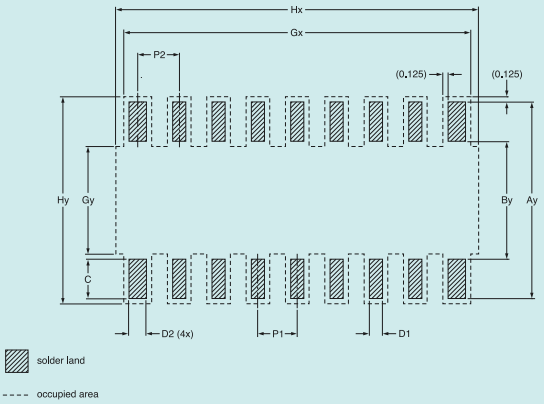
Package dimensions



Dimensions in mm

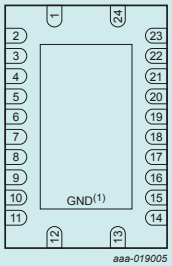
15-05-27

Solder footprint

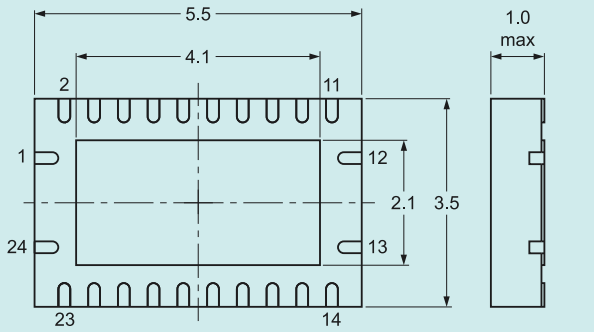


SOT815-1 BQ

Pinout



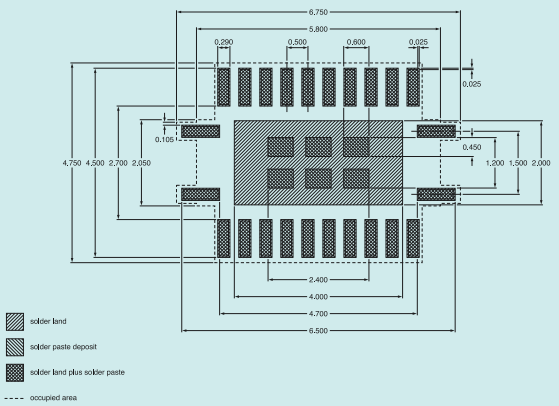
Package dimensions



Dimensions in mm

15-05-26

Solder footprint



Design tools

NXP is committed to making the design process as easy as possible. We offer a range of design tools that make it easier to select the right product for a design, verify performance, explore functionality, and begin prototyping. The result is a smoother development process, and faster time-to-market.

This section includes the following:

- Breakout boards for use with breadboard sockets
- Evaluation boards for standard and configurable logic
- Demo board for AXP configurable logic
- Packaging linecard

How to order

To order a breakout board, an evaluation board, or a package linecard, contact your local NXP sales office or distributor (www.nxp.com/about/sales-offices-distributors), or NXP technical support (www.nxp.com/technicalsupport).

The 74AXP1G57 demo board can be ordered online, at www.nxp.com/logic.

Breakout boards for use with breadboard sockets

Using breadboards is a quick way to create prototypes or experiment with a device, but today's small-scale packages don't always fit in breadboard sockets. NXP's breakout boards are compact PCBs that convert the latest, smallest leadless packages into bigger DIP sockets, providing easy access to all the device I/O.

- TSSOP, PicoGate, MicroPak, DQFN
- Accommodate packages with 5, 6, 8, 10, 12, 14, or 16 pins/pads
- Test pins available for supply pins, I/O access, and measurement
- Coated with solder paste, for easy mounting
- Pre-assembled versions available with specific functions

Breakout boards

GEN1 (1.15 x 0.60 inches)			
SOT number	**Package type**	**No. of pins**	**Pitch (mm)**
353	TSSOP	5	0.65
753	SO5	5	0.95
363	TSSOP	6	0.65
457	TSOP6	6	0.95
886	XSON6	6	0.50
891	XSON6	6	0.35
505	TSSOP8	8	0.65
530	TSSOP8	8	0.65
765	VSSOP8	8	0.50
833	XSON8	8	0.50
902	XQFN8U	8	0.50
GEN2 (1.10 x 0.60 inches)			
SOT number	**Package type**	**No. of pins**	**Pitch (mm)**
363	TSSOP	6	0.65
457	TSOP6	6	0.95
1202	XSON6	6	0.35
1115	XSON6	6	0.30
96	SO8	8	1.27
996	XSON8U	8	0.50
1089	XSON8	8	0.35
1116	XSON8	8	0.30
1203	XSON8	8	0.35
GEN3 (1.60 x 0.60 inches)			
SOT number	**Package type**	**No. of pins**	**Pitch (mm)**
650	HVSON10	10	0.50
1049	XQFN10U	10	0.50
1160	XQFN10	10	0.40
1174	XQFN12	12	0.40
762	DHVQFN14	14	0.50
402	TSSOP14	14	0.65
763	DHVQFN16	16	0.50
1039	HXQFN16U	16	0.50
1161	XQFN16	16	0.40
GEN4 (1.12 x 0.62 inches)			
SOT number	**Package type**	**No. of pins**	**Pitch (mm)**
1226	XSON5	5	0.48
1340-1	HXSON4	4	0.50
1255	XSON6	6	0.50
1348-1	TDQFN6	6	0.65

Evaluation boards for standard and configurable logic

Our evaluation boards enable quick prototyping by providing access to the I/O and supply-voltage pins. They are a convenient way to verify behavior, confirm static and dynamic characteristics under different loads, compare features, and benchmark against the competition. Each board is equipped for easy test and verification of the device's most important features.

Evaluation boards for standard logic

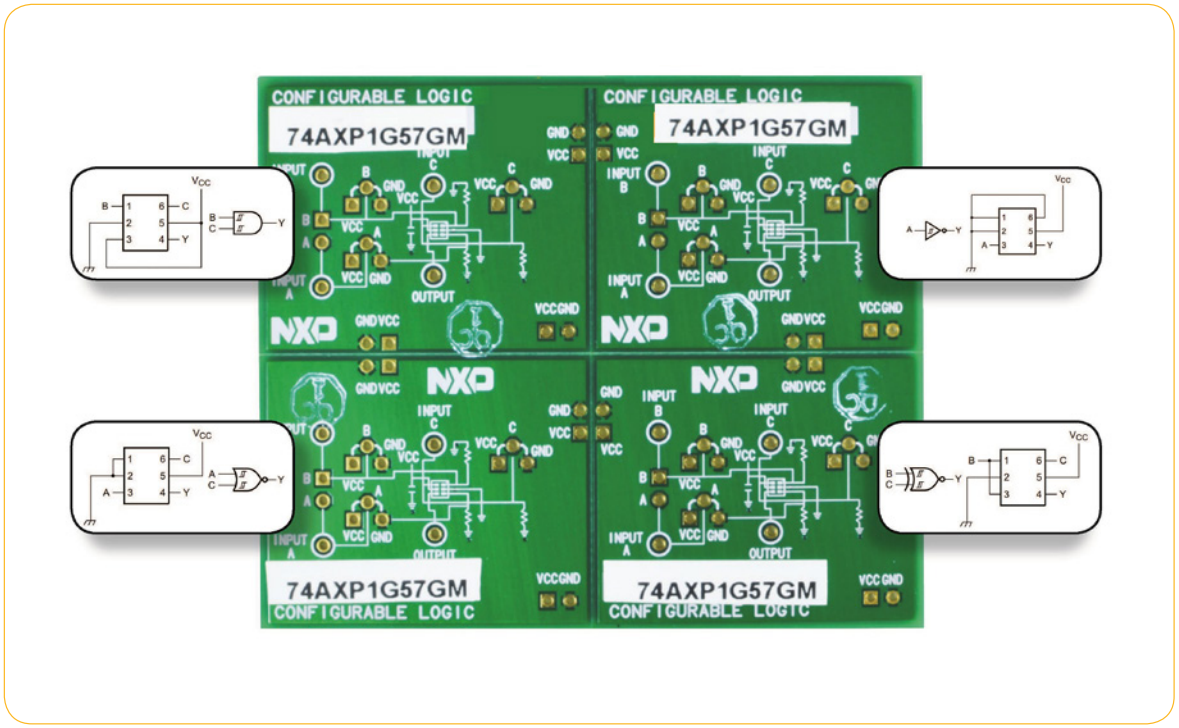
Product number	Description	Board features
74LVC169	Binary counter/ timer	2/4/8/16 clock division, up/down counting
74LVC2G66	Dual SPST switch	Switch high-frequency signals with overvoltage-tolerant control inputs up to 5 V
74LVCV2G66	Dual SPST OVT switch	Switch high-frequency signals with overvoltage-tolerant control and data inputs up to 5 V
74AUP1Z04	Low-power crystal driver	Combines buffered and unbuffered inverters and demonstrates standby mode

Evaluation boards for configurable logic

Configurable logic offers nine or more functions in a single PicoGate or MicroPak package. The pin configuration determines which logic function the device performs, so you can use just one device type to perform multiple functions in your system. Each evaluation board for configurable logic measures just 2.5 x 3 inches, and includes four sections with the same configurable logic device mounted on each section. The user can configure each device to perform one of seven unique functions.

Available for AXP, AUP, and LVC configurable-logic devices

- Power-supply decoupling provided on-board
- Supports external supply voltage of 0.7 to 2.75 V (AXP), 0.8 to 3.6 V (AUP), or 1.65 to 5.5 V (LVC)
- Test points at all I/O pins
- Each board section can be connected or detached via jumpers
- Supports cascading of multiple devices



Evaluation board for configurable logic

Demo board for AXP configurable logic

The AXP1G57GM demo board gives designers a quick, easy way to demonstrate the configurable logic functions.

- Seven 74AXP1G57 devices, each configured as a unique function
- One 74AVC8T245 device, for translation from 1.2 to 3.3 V
- Three push-button switches to toggle the A, B, and C input pins of the 74AXP1G57 device
- NPN transistor PMBT3904 to drive a green/red 2.2 V, 20 mA LED, and a current-limiting resistor
- Rotary switch for selecting one of seven functions with output connected to status LED
- Mini-USB socket or battery holder to supply 4.5 or 5 V DC power to the board

The AXP1G57GM demo board is also available as a sample kit, which includes sample devices, a USB drive with data sheets and other literature, and an optional A-to-B USB cable. The sample kit can be ordered through the e-sample center, located at https://extranet.nxp.com.

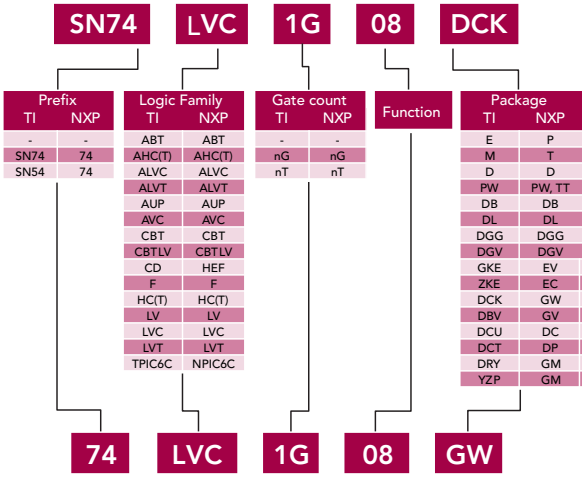
Packaging linecard

NXP offers one of the broadest selections of small-scale, automotive-grade, RoHS-compliant and Halogen-free logic packages. Our packaging linecard, which is populated with actual packages, is a quick reference to compare all our TSSOP, PicoGate, QFN, MicroPak, Diamond, and CSP options. It provides an at-a-glance comparison of size, and lists order number, SOT number, and footprint for each package type.

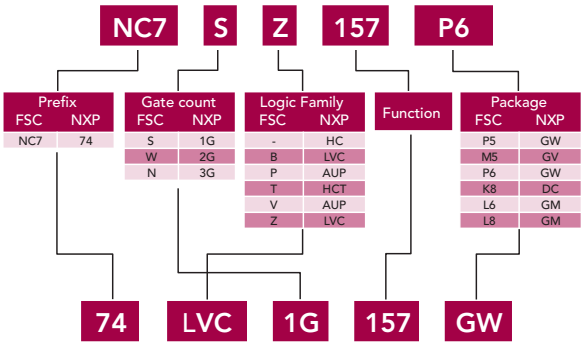
Competitive cross reference

This cross reference allows you to match a competitor's part number to an NXP part number. Once you have the equivalent part number, check the NXP website www.nxp.com/logic to confirm that the particular configuration is released.

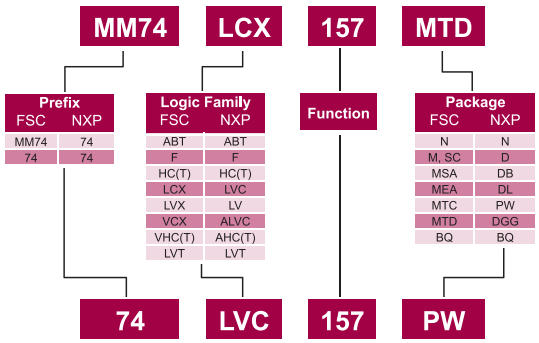
Texas instruments logic



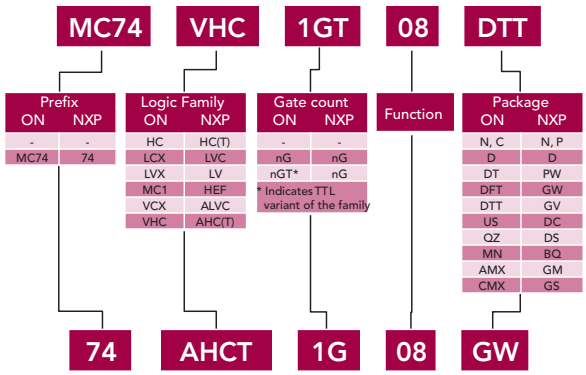
Fairchild semiconductor tiny logic



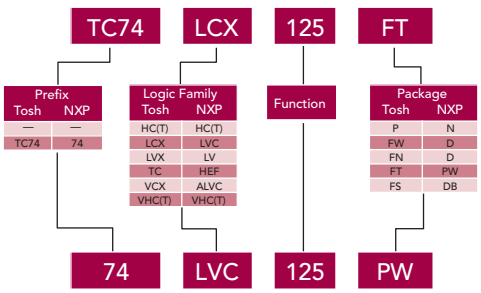
Fairchild semiconductor standard logic



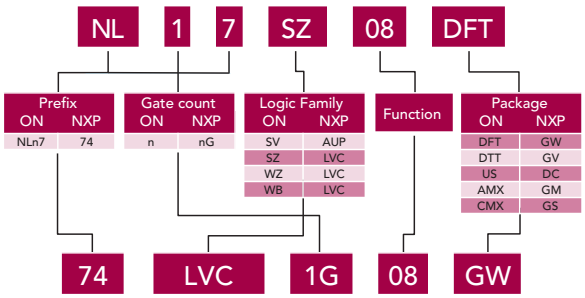
On semiconductors logic



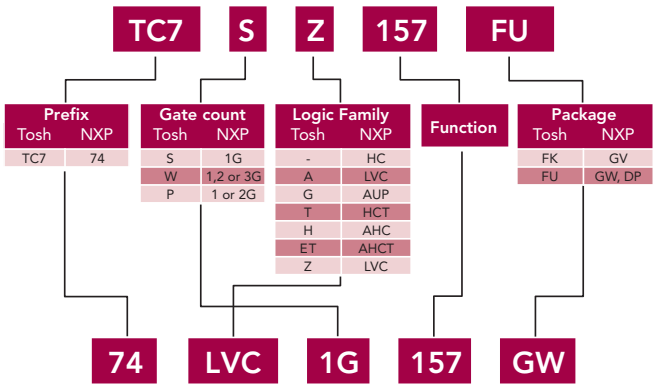
Toshiba standard logic



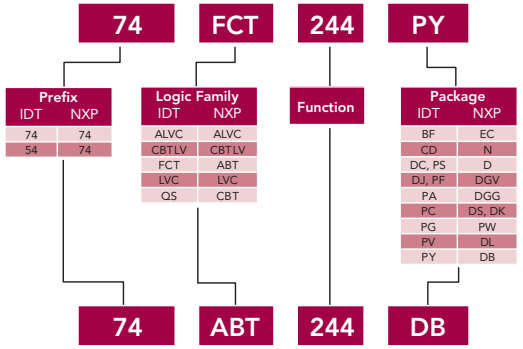
On semiconductor low pin count logic



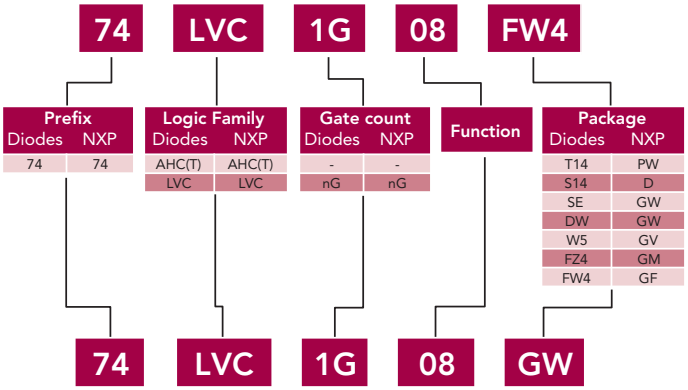
Toshiba one gate



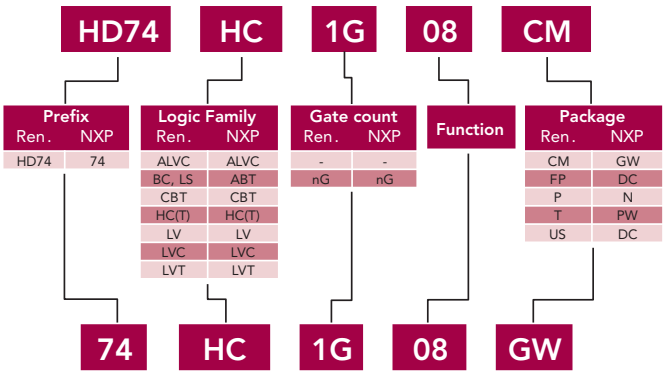
IDT logic



Diodes Inc. logic



Renesas logic



www.nxp.com

Date of release: March 2016
Published in the USA